E3S Web of Conferences **12**, 04004 (2016) DOI: 10.1051/e3sconf/20161204004
i-DUST 2016

Toward an innovative stochastic modeling of electric charges loss through dielectric

G. Micolau[1], J. Postel-Pellerin[2], P. Chiquet[2], M. Joelson[1], C. Abbas[1], D. Boyer[3], and C. Ginoux[1]

[1] UMR 1114 EMMAH, University of Avignon, Department of Physics, Campus Agroparc, 301 rue Baruch de Spinoza, BP. 21239, 84916 Avignon Cedex 9, France
[2] UMR 7334 IM2NP, University of Marseille, 5 rue Enrico Fermi ou 60 rue F. Joliot Curie, Technopôle de Château Gombert, 13453 Marseille Cedex 13, France
[3] UMS 3538 LSBB, La Grande Combe, 84400 Rustrel, France

Abstract. This paper deals with new stochastic modeling of very low tunneling currents in Non-Volatile Memories. For this purpose, we first develop current measurement method based on Floating Gate technique. In order to reach the long time behavior of electrical dynamic, we aim at using very basic tools (power supply, multimeter...) but still having a very good current resolution. Also, our measurement is led in a very particular low-noise environment (underground laboratory) allowing to keep the electrical contacts on the device under test as long as possible. After showing the feasibility of such measurements, we present a modeling approach of the charge loss process inside the Non-volatile Memories by using mathematical tool involving long memory effect. The model is based on stochastic counting process with memory effect yielding to a fractional relaxation equation for the charge loss over time. The main interest of the present model lies in the fact that the corresponding inversion problem involves only two parameters that can be carried out efficiently.

1. Introduction

Flash memory cells are based on the floating gate technology principle [1]. The most widespread solution to enable semiconductor memories to be non-volatile, that is to say able to keep information without any power supply, is to use MOS transistors whose threshold voltage is shifted by a charge stored in an isolated gate above the channel. Floating gate technologies consist in adding a second gate between the gate and the channel of a classical MOS transistor. This second gate can isolate charges to make the transistor threshold voltage variable. Most of the time, charges are injected through a dielectric, in general Silicon dioxide SiO_2, placed between the floating gate and the transistor channel, as presented in Fig. 1. Lastly, the two gates of this "transistor" are separated by another dielectric, most commonly a tri-layer stack oxide "Oxide/Nitride/Oxide" (ONO). Thus, the Flash elementary cell, constituted by a floating gate transistor called "state transistor", can be seen as a classical MOS transistor whose gate would be in series with a capacitor C_{pp}. This gate, called "Floating Gate" (FG), can now store a charge while the second electrode of the capacitor becomes the "Control Gate" (CG) of the cell.

Barrier transparency in the tunnel oxide, which can be electrically modeled by a current source I, allows the injection of charges in the floating gate, shifting the MOS transistor

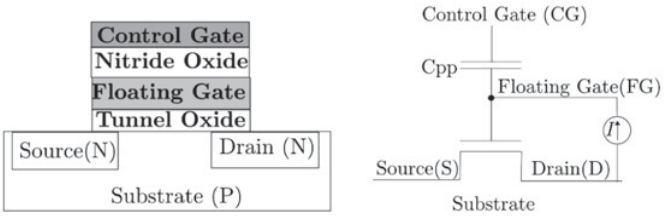

Figure 1. Schematic of a floating gate structure (left) and its electrical scheme (right).

threshold voltage V_T according to (1):

$$\mathbf{V_T = V_{T0} - \frac{Q_{FG}}{C_{pp}}} \tag{1}$$

where V_{T0} is the natural threshold voltage of the cell, Q_{FG} the charge amount in the floating gate and C_{pp} the capacitance between the control gate and the floating gate.

A quantity of charge Q_{FG} is injected into the floating gate by using an adequate set of biases, depending on technology (Flash or EEPROM) [2–5]. Memory cell reliability, defined as the capability of said device to function over time, is a major issue for manufacturers and can be related to many parameters such as process and using conditions. Indeed, unceasing device scaling, decrease of dielectric thicknesses around the floating gate and high voltages applied on cells are many parameters altering memory reliability [6].

Thus, dielectrics' quality is a major issue due to their antagonistic roles: avoiding electric charge leakage currents during retention phase while being transparent enough during programming steps. A better understanding of these leakage currents is crucial to improve the whole quality of our memory cells, that's why we have to develop powerful methods to reach very low current levels.

The "Floating-Gate Technique" (FGT) is generally used and will be detailed in the next section [7, 8]. Using this method requires i) protecting the wafer from mechanical perturbations (vibrations) and ii) (very) long time acquisition. In a classical laboratory environment, those two constraints are generally not easy to deal with. Indeed, they lead to use, for a very long time, huge, heavy and very expensive probers (mechanically insulated by air shocks), which is often economically not possible. The main idea of our experimental platform consists in developing a "cheap" platform. The mechanical insulation is "naturally" done by the very peculiar environment of the underground LSBB Laboratory located in Apt (South of France), presented in Sect. 3.

The second part of the paper is devoted to the presentation of a fractional relaxation modeling to describe the time evolution of the charge loss through the dielectric. As we will see, the main reason to need to model charge loss dynamic lies into the fact that the direct numeral derivation of this latter yields to an unusable leakage current. In the other hand, classical electrical models namely the Fowler-Nordheim and Poole-Franckel are inoperative to model data at the very low range value of leakage current encountered in this work.

2. Floating Gate Technique (FGT)

Most of the electrical measurements developed to characterize semiconductor devices and especially Non-Volatile Memories are based on current measurements. Indeed, to study a major reliability aspect of these NVM we have to evaluate the very low-level leakage currents responsible for the charge loss during the retention phase. Nevertheless, these currents are

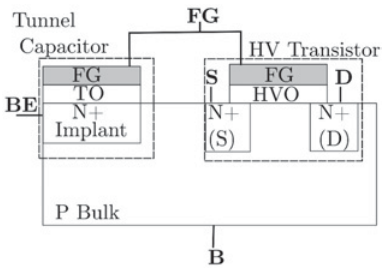

Figure 2. Floating-Gate test structure.

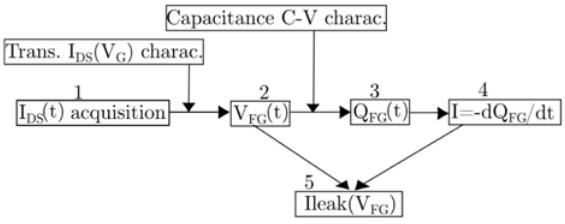

Figure 3. The five key points of Floating-Gate Technique methodology to extract leakage current.

not accessible through direct measurements, even with high-performance analyzers [9], so we have to use some indirect measurement techniques to reach lower level currents. One of the most widely used technique is the "Floating-Gate Technique" (FGT), based on the use of a MOS capacitor and a MOS transistor in parallel [7, 8].

A. Floating-Gate test structure

The Floating-Gate test structure, presented in Fig. 2, consists in a large High-Voltage transistor whose gate is common with the Top Electrode of a large tunnel capacitor, denoted C_{tun}. This common gate plays the role of the Floating-Gate in a memory cell but is directly accessible to apply biases. Tunnel capacitor represents the injection zone of the memory cell. Indeed it has exactly the same process conditions as the injection region (oxide thickness, doping conditions...).

B. Floating-Gate Technique methodology

The Floating-Gate Technique (FGT) is based on the voltage measurement of an initially charged gate of a MOS capacitor, which is then disconnected from the external circuit during the experiment. The measurement of this slowly decreasing gate voltage is performed indirectly through the measurement of the drain current of the transistor sharing its gate with the capacitor. This transistor "converts" the charge of the capacitor, and thus the gate voltage, in a measurable drain current. The temporal variation of this drain current is directly linked to the variation of the gate voltage and thus to its gate charge which is the same as the capacitor charge. Figure 3 depicts the full methodology allowing to obtain the leakage current I_{leak} as a function of the Floating-Gate voltage V_{FG}.

The extraction methodology requires two preliminary characteristics, the $I_{DS}(V_{FG})$ characteristics of the transistor and the C-V curve of the tunnel capacitor, presented in Fig. 4.

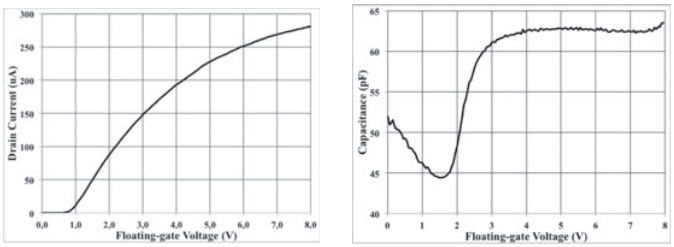

Figure 4. Preliminary characteristics required in the leakage current extraction: $I_{DS}(V_{FG})$ (left) and C_{tun}–V_{FG} (right).

The Floating-gate voltage is the image of the Floating-Gate charge Q_{FG}, extracted from the $C_{tun}(V_{FG})$ characteristics, presented in Fig. 4, using (2):

$$\mathbf{Q_{FG}} = C_{\mathbf{tun}} \times \mathbf{V_{FG}}. \tag{2}$$

The leakage current I_{tun} is then the variation of this Floating-gate charge Q_{FG} over time (3):

$$\mathbf{I_{tun}} = -\frac{\mathbf{dQ_{FG}}}{\mathbf{dt}} \cdot \tag{3}$$

To reach very low-level currents, we have to acquire the drift of the transistor drain current over very long time, keeping applied biases on the transistor (except on the Floating Gate) during the whole experiment. The main difficulty is to keep the electrical contacts on the device under test for days, weeks or even months, knowing the longer the measurement, the lower the extracted current. When using classical probe stations, it is difficult to keep electrical contacts for more than a few days due to the ambient vibrations [10]. Electromagnetic perturbations also disturb the experiment due to the very slow drift of the drain current we have to measure. All the existing solutions to enable a long drain current acquisition lead to very heavy and expensive test bench that we propose to avoid in our study. The improvement consists in developing a cheap but very sensitive test bench, embedded in a particular environment.

3. Low-noise environment

To reach very low levels of electrical and mechanical noises, we have first chosen a specific test environment with a very low electromagnetic noise and a very low vibration level, allowing to use a very simple test bench.

3.1 Specific test environment: The Low Noise Underground Laboratory of Rustrel

The Low Noise Underground Laboratory in Rustrel Pays d'Apt (South of France) is a set of horizontal galleries dug in the bedrock of Big Mountain, bordering South Albion plateau. It was dedicated to be the former cockpit shooting # 1 of the French nuclear deterrent force, from 1973 to 1998. It was built to resist a nuclear weapon assault. It allows access to different rooms (for a total of 14,000 m^2) along 3.7 km, in a rock cover varying from 30 to 519 m under the Surface topography. Rooms and galleries are shielded (electromagnetic waves), by concrete and massive steel shields. This peculiar environment is now used by the National Institute of Universe (INSU) as a hydrogeological, geophysical (net of seismographs) and astronomical (muons detectors) observatory since few years. It also allows to test microelectronic devices in a non radiative environment. For our purpose,

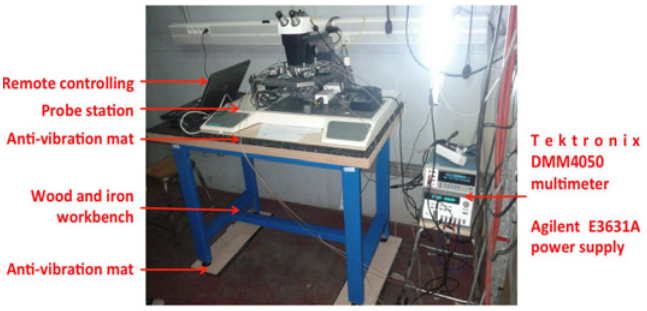

Figure 5. Picture of the proposed test bench, embedded in the low-noise environment.

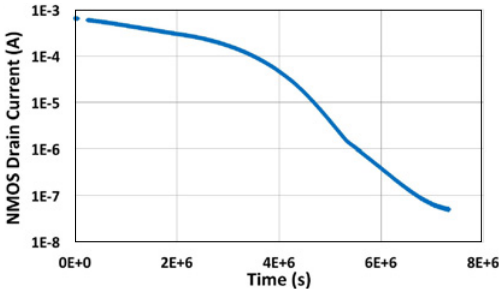

Figure 6. Acquisition of the drain current of the NMOS transistor for an initially positively charged tunnel capacitor.

this laboratory is the "perfect environment" since it allows to avoid electromagnetic and mechanical perturbations during a very long time range. Our platform has been installed at the end of the gallery, where the perturbations are supposed to be the smallest.

3.2 Proposed test bench

Our experimental platform is based on a classical probe station with 5 manipulators and needles, an Agilent E3631A triple output DC power supply and a Tektronix DMM4050 digital multimeter, as illustrated in Fig. 5. To avoid as much as possible any movement around the test bench, a fully remote controlled experiment has been performed. The complete description of the test bench is given in [11] and improvements in the robustness of the technique can be found in [12].

3.3 Instance of experimental results

The experiment exposed here has been successively performed on a NMOS Floating-Gate test structure. The drain current drift acquisition over time (up to almost three months) is shown in Fig. 6.

By applying the methodology detailed in Section II.B and using preliminary characteristics from Fig. 4, we can obtain from the evolution of the capacitor charge Q_{FG} (Fig. 7a) and the extracted leakage current (Fig. 7b) over time.

As a first comment from Fig. 7a, we note that at time around t = 2.5e6 sec. a slope break on the charge behavior appears clearly. This suggests the presence of two schemes of the charge decrease. As observed in Fig. 7b, the curve of the leakage current from direct

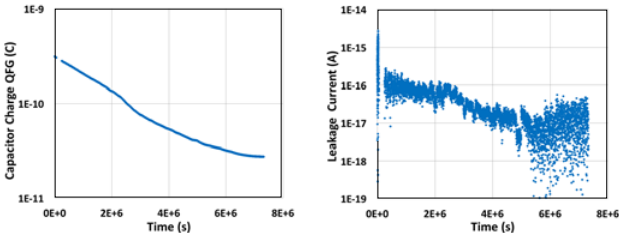

Figure 7. Extracted a) capacitor charge and b) leakage current, on NMOS.

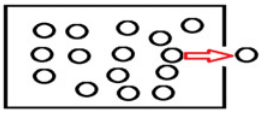

Figure 8. Charges trapped in the dielectric may be seen as a sample of moving particles inside a box with an opening to the outside.

derivative of charge evolution is found to be highly noisy and is not suitable to define a clear trend for current leakage. More precisely, this means that the charge loss curve does not possess the required mathematical derivability properties. This is related to a more deeply reason involving the fact that process causing charge particle to come out the dielectric medium is probabilistic. As a consequence, it is necessary to model the charge evolution curve as a relaxation law of random process.

4. Modeling electric charge dynamic

4.1 Relaxation model

The simplest model of relaxation phenomenon is given by the exponential law. To illustrate it, let us consider that electrons (charges) may be seen as a sample of moving particles inside a box with an opening to the outside.

Then, measuring charge evolution inside the dielectric is equivalent to counting number of remaining particles. Let q(t) the probability that one particle will come out of the box during time interval [0,t[. In addition,one can make the assumption that the output probability q (t) do not change with the number ofremaining particles. In other words, there is no memory effect on the random process. This is the *Poisson process* for which, the probability to have N particles at time t is given by

$$(N,t) = \frac{(kt)^N}{N!}\exp(-\mathrm{Ct}). \tag{4}$$

In this case, it is well-known that the survival probability q(t) writes as:

$$\mathrm{q(t)} = 1 - \exp(-\mathrm{Ct}). \tag{5}$$

The parameter C is the probability that a given particle is instantaneously out side the box. Also, the number of particles inside the box will be a random process N(t) following a binomial law and then the mean value n at time t follows ordinary differential equation

$$\frac{d}{dt}n\,(t) + Cn\,(t) = 0. \tag{6}$$

Obviously, the solution is given by an exponential law

$$n(t) = \mathrm{n}_0 \exp(-\mathrm{Ct}) \tag{7}$$

where n_0 is the initial number of particles. It is a memory less relaxation law, known also as the desintegration law.

4.2 Relaxation with Memory Effect

If memory effect is taken in account *i.e.* the probability of particle to come out is now depending on the number of remaining particles, then we have a Fractional Poisson Process [16] and the probability P(N,t) is given by

$$\begin{cases} P(N,t) = \frac{(-t)^N}{N!} \frac{d^N}{dz^N} E_{\alpha,1}(\mathrm{z}) \Big| \\ P(N=0,t) = E_{\alpha,1}(-(\mathrm{Ct})^\alpha) \end{cases} \mathrm{z} = -(Ct)^\alpha . \tag{8}$$

Where $E_{\alpha,\beta}(\mathrm{z})$ is the Mittag-Leffler function [18] defined as:

$$E_{\alpha,\beta}(\mathrm{z}) = \sum_{m=0}^{\infty} \frac{z^m}{\Gamma(\alpha m + \beta)} \quad \alpha > 0 \text{ and } \beta \in \mathbf{C} \tag{9}$$

with $\Gamma(\mathrm{t}) = \int_0^\infty x^{(t-1)} e^{-x} dx$ is the Gamma function. The Mittag-Leffler function is a generalization of the exponential function with $E_{1,1}(\mathrm{z}) = \exp(\mathrm{z})$. The real α is the fractional order of the process. The mean value n of number of particles at time t follows the fractional relaxation equation

$$\frac{d^\alpha}{dt^\alpha} n(t) + Cn(t) = 0. \tag{10}$$

Where $\frac{d^\alpha}{dx^\alpha}$ is the fractional Caputo derivative of order α defined as:

$$\frac{d^\alpha f}{dx^\alpha}(x) = \frac{1}{\Gamma(1-\alpha)} \int_0^x (x-\xi)^{-\alpha} \frac{df}{d\xi} d\xi, \qquad 0 < \alpha \leq 1.$$

Equation (10) is known to have analytic solution in term of Mittag-Leffler function [17]. In which follows, we will use solutions of the model Eqs. (6) and (10).

5. First result

5.1 Curve fitting

In the Fig. 6, we present the result of fitting procedure of the data experiment with the two relaxation models as presented in former section. The fitting method was carried out by optimization of a cost function measuring the distance between experimental data and models defined as:

$$F = ||n - Q_{FG}||_2. \tag{11}$$

The Levenberg-Marquard algorithm is used in order to produce the parameter C for the exponential model and the parameters (α,C) for the fractional relaxation. In this case, two fits results are proposed. The first corresponds to the upper part of the data experiment decreasing while the second fits the lower part of the data corresponding to long time behavior.

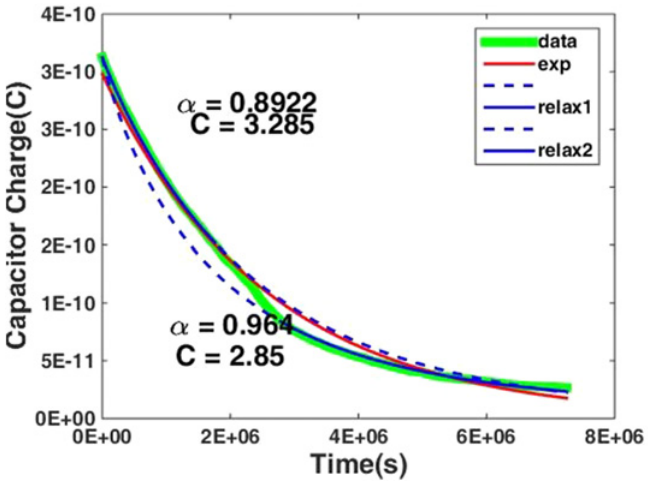

Figure 9. Different Relaxation models of charge loss (Dashed line indicates part of the M.F. approaches which does not fit the data dynamic).

5.2 Comments and discussions

Firstly, we note that the regime change observed in the section appears as the threshold region of the two schemes of fractional relaxation. We remark also that the exponential model used to fit the whole range of data does not match with this latter around this region. In the other hand, similar behavior is found for both fractional relaxation laws. These results suggest that two separate schemes may exist at two different time scales. Such conclusion has to be confirmed by the analysis of other datasets. If the result holds, we believe that an unified model is essential to depict the dynamic evolution of the charge loss over time. This may be reached by use of more complex random physical models such as anomalous diffusion process which takes account of possible long time trapping of particles inside the medium. Among, the possible candidates, we think that fractional Mobile Immobile model could be a suitable candidate.

In this case the main idea is to enforce a stochastic model that uses few parameters to describe charge transit through the oxide as a random walk. This approach to charge transport tentatively allows, from a macroscopic point of view, to link the observed evolution laws to dispersive (and possibly fractional) transport models [13]. This kind of models has been successfully used for mass transit through complex porous systems [14] as wells as other diffusive phenomena [15].

From electrical viewpoint, two complementary physical theories are known to describe these two schemes of current leakage behavior, namely the Fowler Nordheim (F-N) and the Poole Frankel (P-F) currents. The F-N current corresponds to a leakage process that appears at large value of floating gate voltage (VFG>3V) while the P-F current known also as the trap assisted tunneling current is predominant at low voltage range. As said in introduction, owing to the fact that these electrical models cannot be reached at very low current values, a valuable task for the future is to link our stochastic modeling that is easily available from datasets, with these electrical models (F-N and P-F).

6. Conclusion

Using classical protocol of the Floating Gate measurement, we are developing a new model of charge loss. Works still in progress. The main interest of our model comes from its robustness

requiring only few parameters. In the other hand, electrical models of P-F and F-N need efficient leakage current measurement that cannot be reached from numerical derivation of charge loss data. In this context, our stochastic model allows one to derive the charge loss dynamic in a statistical sense.

References

[1] W. Brown and J. Brewer, "Nonvolatile semiconductor memory technology: a comprehensive guide to understanding and to using NVSM devices," IEEE Press, 1998.

[2] P. Canet, R. Bouchakour, N. Harabech, P. Boivin and J.-M. Mirabel, "Eeprom programming study-time and degradation aspects," Proc. of IEEE ISCAS, pp. 846–849, 2001.

[3] R. Laffont, R. Bouchakour, O. Pizzuto and J.-M. Mirabel, "A 0.18 um flash source side erasing improvement," Proc. of IEEE NVMTS, pp. 105–109, 2004.

[4] P. Canet, R. Bouchakour, N. Harabech, P. Boivin, J.-M. Mirabel and C. Plossu, "Study of signal programming to improve eeprom cells reliability," Proc. of IEEE MWSCAS, pp. 1144–1147, 2000.

[5] P. Canet, R. Bouchakour, J. Razafindramora, F. Lalande and J.-M. Mirabel, "Very fast eeprom erasing study," Proc. of IEEE ESSCIRC, pp. 683–686, 2002.

[6] ITRS, "Process Integration, Devices, and Structures", 2013.

[7] B. Fishbein, D. Krakauer and B. Doyle, "Measurement of Very Low Tunneling Current Density in SiO, Using the Floating- Gate Technique," IEEE Elec. Dev. Lett., **12**, no. 12, pp. 713–715, 1991.

[8] F.H. Gaensslen and J.M. Aitken, "Sensitive Technique for Mea- suring Small MOS Gate Currents," IEEE Elec. Dev. Lett., **1**, no. 11, pp. 231–233, 1980.

[9] Keysight B1500A Semiconductor Device Analyzer data sheet, October 2016.

[10] S. Burignat, "Mécanismes de transport, courants de fuite ultra-faibles et rétention dans les mémoires non volatiles à grille flottante," PhD thesis, INSA Lyon (France), 2004.

[11] J. Postel-Pellerin, G. Micolau, P. Chiquet, J. Melkonian, G. Just, D. Boyer and C. Ginoux, "Setting up of a floating gate test bench in a low noise environment to measure very low tunneling currents," Acta Imeko, **4**, no. 3, pp. 36–41, 2015.

[12] J. Postel-Pellerin, G. Micolau, C. Abbas, P. Chiquet and A. Cavaillou, "Robustness of the floating-gate technique in a very low-noise environment," Proc. of IEEE CAS, pp. 287–290, 2014.

[13] M.-C. Néel, A. Zoia, M. Joelson, A. Cartalade and M. Fleury, "Fractional p.d.e and stochastic processes for dispersion: application to porous media," Proc. of "Dynamiques fractionnaires et Applications" Conference, 2010.

[14] J. Golder, M. Joelson and M.-C. Néel, "Mass transport with sorption in porous media," Mathematics and Computers in Simulation, **81**, pp. 2181–2189, 2011.

[15] J. Golder, M. Joelson, M.-C. Néel and L. Di Pietro, "A time fractional model to represent rainfall process," Water Sci. and Engineering, **7**, no. 1, pp.32–40, 2014.

[16] N. Laskin, "Fractional Poisson Process" Communication in Nonlinear Science and Numerical Simulation, **8**, pp. 201–213, 2003.

[17] D. Sierociuk, I. Podlubny and I. Petras "Experimental Evidence of Variable-Order Behavior of Ladders and Nested Ladders". IEEE Transactions on Control Systems Technology **21**(2), 2011.

[18] Kilbas AA, Saigo M, "Generalized Mittag-Leffler function and generalized fractional calculus operators". Integral Transform Spec. Func. **15**(1):31–49, 2004.