VERY HIGH FREQUENCY POWER SWITCHING: A ROAD MAP TO ENVELOPE TRACKING

Christophe Delepaut [(1)], Natanael Ayllon [(2)]

(1) ESA/ESTEC, Keplerlaan 1, 2201 AZ Noordwijk, The Netherlands, Email:Christophe.delepaut@esa.int
(2) ESA/ESTEC, Keplerlaan 1, 2201 AZ Noordwijk, The Netherlands, Email:Natanael.Ayllon@esa.int

ABSTRACT

RF (Radio Frequency) GaN transistors may be used for power switching at frequencies of 30 MHz and above, thereby reaching voltage control bandwidth of critical interest for the so-called ET (Envelope Tracking) technique. ET is meant at optimising the efficiency of RF amplifiers by supplying them with a voltage adapted to their power level at any time, and is the subject of many R&D works worldwide. The present paper provides an overview on the different activities run at the European Space Agency so far in this context, and present the possible way-forward to embark ET on future spacecraft.

1. INTRODUCTION

Power switching for space applications typically features Si MOSFET (Silicon Metal Oxide Semiconductor Field Effect Transistor) run at frequency of some hundreds of kHz. The applicable power levels stretch from a few W up to tens of kW, and the voltage levels from a few V to hundreds of V [1][2]. Such characteristics are driven by the ON serial resistance time parasitic capacitance FoM (Figure of Merit) of the concerned semiconductor technology which relates to the losses in conduction and in switching.

The emergence of the GaN HEMT (Gallium Nitride High Electron Mobility Transistor) technology for switching has recently resulted in significant improvement of both switching and conductive losses, allowing power switching to be operated in the low MHz region at fair conversion efficiency for similar voltage levels [3][4].

The above-mentioned state-of-the-art switching FET (Field Effect Transistor) are so-called “normally OFF”, i.e. open at zero gate to source voltage, and have a positive commutation threshold voltage with respect to drain polarity. To this extent, they oppose to GaN HEMT meant for RF amplification which are “normally ON” and have a negative commutation threshold.

RF GaN FET have even more reduced parasitic capacitance with respect to its counterpart for switching, and may be used for switching, however at a price of appropriate gate biasing (negative voltage for N-FET). Such technology opens the way to switching at VHF (Very High Frequency), namely 30 MHz and above, for targeted voltage levels of up to 100 V [5]. This in turn enables voltage control bandwidth in the 10 MHz region.

On the other hand, payloads of power switching units within spacecraft encompass RF amplifiers, called transmitters, for communication or broadcasting purpose. Such amplifiers dissipate all the more power that their RF output power is low. To lower the dissipated power, an effective mean consists in supplying them with a voltage modulated proportionally to the signal envelope amplitude. Such technique is called ET (Envelope Tracking). Relevant amplitude modulation bandwidths are application dependent, with a low end starting at 10 MHz [6].

Accordingly, VHF power switching may match the requirements for ET. In this context, ESA started its own investigation and placed a number of Contracts with University, Scientific Institute and Industry. The present paper reports the results achieved in the different Contracts so far, and how they fit within an overall ET road map. It supports and highlight the way-forward towards a full scale Industrial application of ET on board of spacecraft.

The paper is organised as follows. Chapter 2 deals with background information on ET and describes the main building blocks. Chapter 3 addresses the most significant past and ongoing Contracts placed by ESA and synthetises their outputs. In Chapter 4, the road map is exposed. The TRL (Technology Readiness Level) of the different technologies involved is identified, and an overview is provided with a GANTT chart. Conclusions are delivered in Chapter 5.

2. BACKGROUND INFORMATION

2.1 Overview

Nowadays, there is a raising interest in using complex and high order digital modulation schemes with high spectral efficiency in order to achieve high amounts of data rate needed for high demanding services. The counterpart of using these high order modulation schemes is the inherent high PAPR (Peak to Average Power Ratio) of the telecommunication signal, which means that there is a large difference between the average amplitude and the peak amplitude of the signal.

Common space-borne transmitters based on SSPA (Solid State Power Amplifiers) use static supply voltages to the RF transistors. In order to have a high efficient transmitter (required for space-borne applications where the DC power available is limited), the high power amplifier needs to be operated close to saturation. However, if the signal to be transmitted has large PAPRs, this will mean that the signal is clipped and heavily distorted. The consequence is a transmitter able to provide the required amount of power, but with a very distorted shape that is not often possible to correctly demodulate in Ground. Therefore, the link is not usable.

The solution to this point is indeed to reduce the operating point to a more linear region so that the amplification is done in a more linear manner. The consequences are lower output power transmitted and a low efficient transmitter. If the DC power supply is static, the power consumption will keep high while the RF output power is decreased. This translates into higher power to be dissipated, directly impacting the reliability of the components on-board the SSPA.

Generally speaking, linearisers are able to pre-distort the signal to compensate for the distortion introduced by the SSPA. Therefore, the operation of the transmitter can become closer to the saturation area, making the transmitter more efficient with a lower signal distortion. Nevertheless, the solution is not flexible and optimum enough against dynamic changes of the modulation scheme or changes in the RF output power, as it is required today in many flexible payloads. In this context, ET can enable a step forward to achieve high level of RF output power flexibility together with high level of efficiencies.

ET is a high efficiency amplifier architecture that consists of extracting the envelope information from the RF carrier, amplify it and supply this envelope to the drain or collector of the high power RF transistor in the RF path, as shown on Fig. 1. This is often called a dynamic supply architecture.

The main benefit of this architecture is that the transmitter is able to keep high levels of efficiency at levels of input power back off of several dBs (up to 10dB). Therefore, in presence of complex and high order digital modulation schemes with significant PAPR, the transmitter operates at high level of efficiency almost all the time.

With the advent of Gallium Nitride technology for the RF devices, the interest for this high efficiency SSPA architecture has even raised.

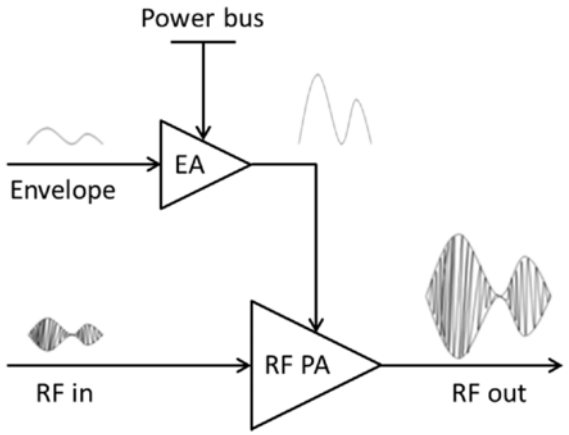

Figure 1. ET-SSPA architecture [5]

The reason is that RF GaN amplification transistors are potentially able to operate at different supply voltage levels without significantly changing the optimum output impedance. This means that a dynamic supply modulation scheme can be applied, guaranteeing optimum operation of the RF amplifier at all bias supply levels. This is particularly important for guaranteeing a good stability of the RF power amplifier, preventing it from undesired oscillations during the supply change.

2.2 Building Blocks

As depicted in Fig. 1, the ET-SSPA has two main building blocks. The first and most important one is the EA (Envelope Amplifier), that is in charge of acquiring the envelope of the RF signal and amplify it to the right level of voltage required by the RF Amplifier.

For space-borne SSPAs targeting L/-S- applications the EA should be able to be fed by 100V bus voltage and should be able to provide voltage variations in the order of 20 to 50 V with current values of 2 to 4 A. All this should be achieved with DC power conversion efficiency in the order of 90 %. At the same time, the EA should be able to smoothly amplify envelope signals with large bandwidth, that is, with very fast time domain response.

Additional requirements for the EA encompass high gain of typically 40 dB, high linearity, low noise, including low switching ripple, and high slew rate capability, in the order of 1 V/ns, as the bandwidth performance must be met not only for small signals but also for large signal variations.

The second key building block is the RF power amplifier. What changes in an ET-SSPA from a standard class-AB amplifier is that now the RF amplifier operates with dynamic drain voltage supply. In addition, the drain bias network typically designed for the RF amplifier now interfaces with the output filter

of the DC/DC converter of the EA. This is an interesting feature that brings a difficult trade-off: bandwidth of the output filter versus output ripple of the overall ET-SSPA.

3. R&D CONTRACTS AT ESA

3.1 Envelope Amplifier

In 2011, a 3 year long NPI (Networking/Partnering Initiative) Contract has been placed with the University of Mons and the support of TAS (Thales Alenia Space), in Belgium, to demonstrate the feasibility of VHF power switching meant as EA (Envelope Amplifier) for ET applications.

The targeted converter was based on a step down Buck topology. The converter is provided with the envelope reference extracted from the input RF signal and must deliver the amplified envelope with the appropriate gain. A step down topology is appropriate for spacecraft power bus regulated at 50 V or 100 V.

The converter output voltage was to be controlled in closed-loop. There are several reasons why such feedback loop is implemented. First, it ensures a better input to output linearity with respect to component drift and non-linearities. Secondly, it also allows the converter output filter to have a cut-off frequency lower than the control bandwidth. This is desirable as the output voltage ripple must be kept low without compromising the tracking bandwidth. Finally, placing the output filter cut-off frequency within the control bandwidth makes possible active damping of the filter with no dissipative resistor.

From a practical viewpoint, the Buck converter has been implemented in a reverse configuration, meaning that the switching FET is grounded and that the rectifying diode is connected to the supply voltage. Accordingly, the load is to be connected between the power supply and the converter output. The asset of the reverse buck is that its switching operation is much easier as the FET gate source dipole is no longer floating as in a normal FET, which feature may prove critical at VHF. On the other hand, the accommodation of the RF amplifier with the reverse Buck is not straightforward and is addressed below (see § 3.3).

The manufactured breadboard is shown on Fig. 2. It is constituted by power dice directly mounted on the chassis and low level dice assembled on RF substrate. Input to output power conversion efficiencies well above 90 % have been reached at 50 MHz switching frequency, 50 V input voltage and power level up to 45 W. The efficiency measurements are provided on Fig. 3.

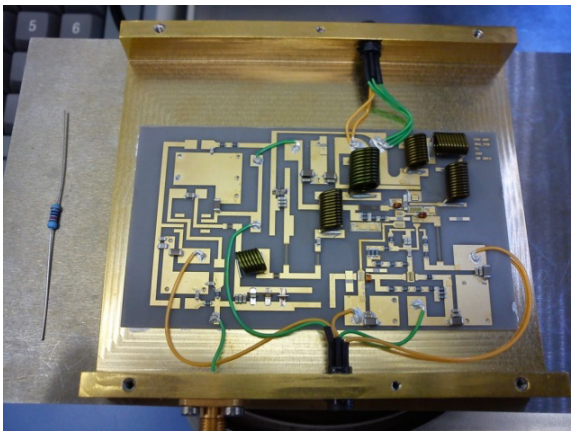

Figure 2. VHF power switching breadboard

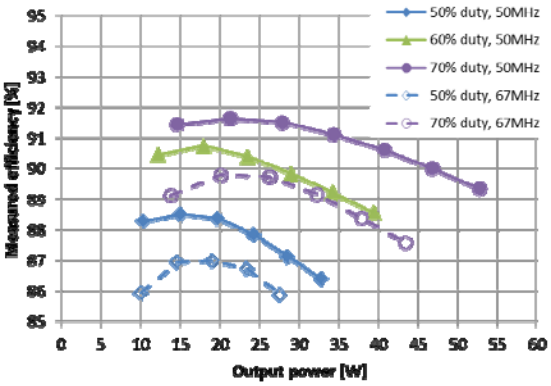

Figure 3. Efficiency at 50 V input voltage

From feedback control viewpoint, the tracking of a 1 MHz envelope reference has been demonstrated, albeit at a price of lowering the switching frequency of the self-oscillating switching controller down to 10 MHz. The tracking measurement is reported on Fig. 4. The large peak to peak switching ripple is a consequence of the lowering of the switching frequency.

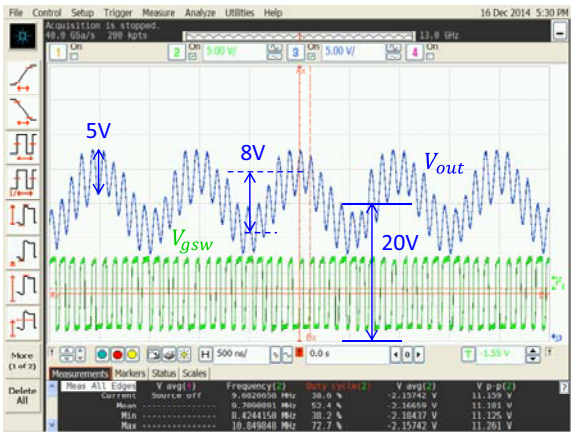

Figure 4. Sine reference envelope tracking

The reason for lowering the switching frequency was the larger than expected open-loop phase shift in function of frequency. This is driven by the choice of a AlN (Aluminium Nitride) substrate selected for its enhanced thermal conductivity desirable for the driver output stage. The drawback of this substrate is its larger dielectric permittivity. Accordingly, the propagation speed of the signal along the tracks was lowered, and the parasitic track capacitance combined with design resistance resulted in stronger parasitic time constant. In both case, the size of the control circuit was critical, which indicates that the integration of the driver circuit is of crucial importance.

3.2 Modulator & Driver Integrated Circuit

In 2015, a 2 year long ARTES 5.1 (Advanced Research in Telecommunications Systems) activity was started with IMST, in Germany. The objective of this Contract is to develop an IC (integrated Circuit) able to drive the switching GaN FET within the EA. The IC is to include not only the FET driver itself, but also modulator which is the circuit in charge of determining the duty cycle to be applied to the switching FET. The modulator & driver function is identified within the ET system diagram on Fig. 5. The closed-loop operation of the EA is not shown on this diagram, but consists in a feedback from the DC/DC converter output towards the modulator input.

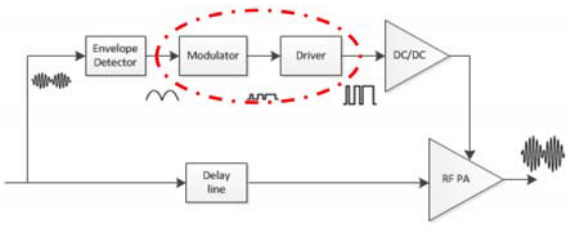

Figure 5. Modulator and driver within ET system

The IC design significantly benefits form the return of experience accumulated during the above-mentioned NPI activity where a discrete modulator and driver design was implemented. As a specific challenge, it has to operate switching up to 100 MHz with peak to peak output voltage of 6.5 V and slew rate of more than 10 V/ns loaded by a switching FET gate capacitance of up to 30 pF.

Two microelectronic technologies have been compared for the design of the circuit, namely the UMS25GH GaN technology and the IHP's SGB25VGD SiGe (Silicone Germanium) one. The trade-off has shown that the SiGe process, combining the advantage of CMOS devices, bipolar transistors and complementary RF LDMOS devices, was superior to the GaN process as to reach the requested output slew rate performance. The technology has been selected accordingly.

The Contract encompasses two successive wafer runs. The intention is to inject into the second wafer run the lessons learned during testing of the first sample. The first wafer of the modulator & driver circuit was designed as two separate dice, as shown on Fig. 6, giving more flexibility from testing and signal accessibility viewpoint. The second and final wafer run will consist in a single die.

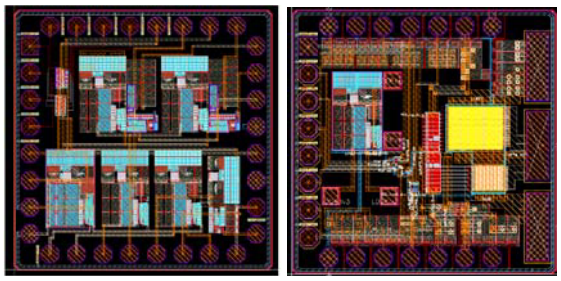

Figure 6. Driver & modulator IC prototype

To demonstrate that the developed IC successfully fits within an EA, the Contractor undertook to design with ESA support a VHF switching converter as test bench to be used to validate the behaviour of the circuit. Relevant simulations of the switching FET gate and drain voltages are shown om Fig. 7.

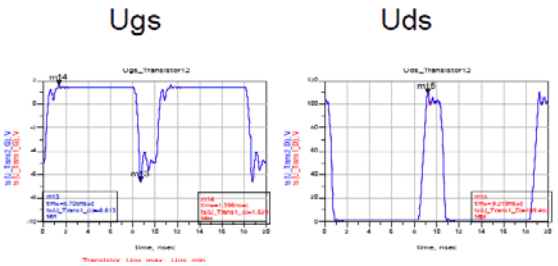

Figure 7. VHF power switching simulation

The targeted power level is 240 W. Simulations indicate an efficiency figure reaching up to 91.7 % at 100 MHz switching frequency. The breadboarding activity is ongoing at the time of writing this paper.

3.3 Envelope Tracking System

By end of 2015, a 2 year long continuation NPI Contract has been set up with FBH (Ferdinand Braun Institute) in Berlin, Germany, and with the support of TAS in Belgium. The focus of this activity is about interfacing the EA with the RF amplifier being the main constituents of the ET system.

The ET system is displayed on Fig. 8, with the EA on the left side, incorporating the reverse buck topology, and the RF amplifier on the right side [7]. The figure highlights that the RF ground is separated from the system ground due to the choice of the reverse buck converter.

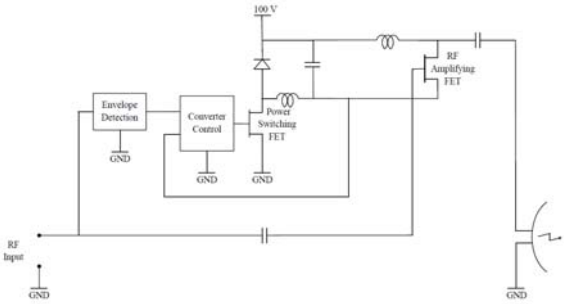

Figure 8. ET system architecture (patent pending)

The benefit of the reverse Buck has been explained earlier (see §3.1). From RF load interface viewpoint, the dedicated RF ground is not an issue due to the capacitor coupling any RF amplifier with its load. Such capacitor is meant to eliminate the envelope voltage before delivering the amplified RF signal.

It is underlined that reversing the Buck has shifted the dV/dt issue from the switching FET source to the RF FET source. However the order of magnitude has been mitigated by a factor three, from about 1 kV/ns on the switching node of the Buck at 100 MHZ switching frequency down to typically 1 V/ns at RF amplifier reference voltage for a 10 MHz tracking bandwidth.

In the frame of the ongoing Contract, an RF amplifier compatible with the above-mentioned architecture has been designed and breadboarded, with convenient attention paid to the in-band and out-band stability. The breadboard is shown on Fig. 9.

The left and right connectors are the RF input and output. The three upper connectors connect the RF FET drain, gate and source. The testing of the amplifier is successful so far [8]. Large signal testing is ongoing.

The RF amplifier is subsequently to be connected to power switching EA. Such configuration will deliver very valuable information on the ET system, including not only overall efficiency performance but also sensibility to switching ripple amplitude, to tracking bandwidth and envelope delay, to residual non-linearities, etc.

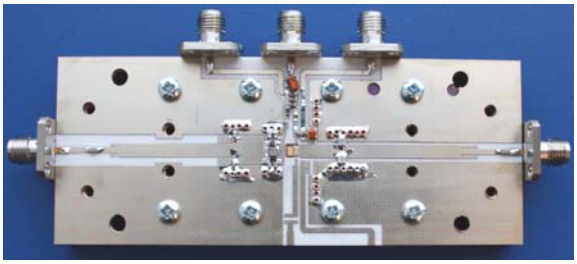

Figure 9. Floating RF amplifier breadboard

Finally, the Contract is going to concentrate on the coupled design of the EA with an RF amplifier, based on the outputs of the previous steps. This last step includes preliminary experimental validation.

4. ROAD MAP

The ESA Road Map is based on activities initiated one decade ago. It concerns the ET system, which encompasses the EA and the RF amplifier. As a critical component, the EA includes the modulator & driver circuit meant for driving the VHF switching operation.

The NPI activity performed with the University of Mons has brought the EA concept, based on a single VHF switching converter, up to TRL3 (Technology Readiness Level).

The ARTES activity with IMST is currently bringing the modulator & driver circuit up to TRL5 by delivering a workable IC chip. The associated validation works at EA level are also bringing the EA concept up to TRL5.

The ongoing NPI activity with FBH is going to bring the whole ET system up to TRL3.

Accordingly, the next activity shall target to increase the maturity level of the ET system from TRL3 to TRL5. All critical functions are to be implemented within an EM (Engineering Model), to be designed, manufactured and tested in a relevant environment.

The Road Map GANTT chart is displayed on Fig. 10. It focuses on year 2016 and beyond. The ongoing ARTES and NPI Contracts are identified, pointing at the future activity for EM development.

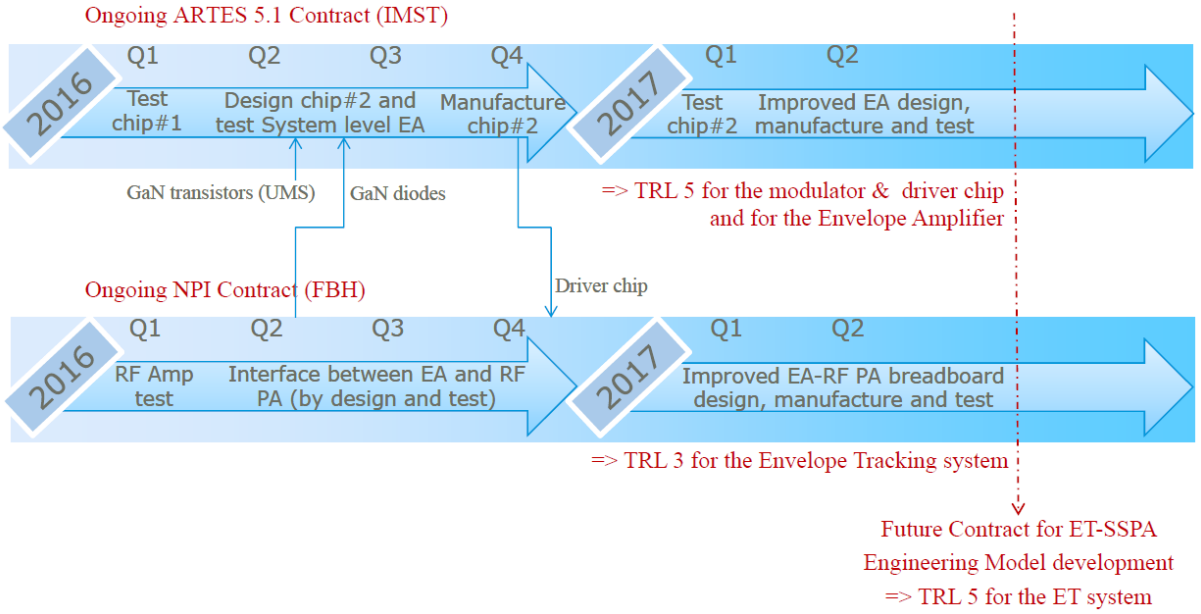

Figure 10. ET road map GANTT chart

5. CONCLUSION

ET is a promising technique to reduce electrical power consumption and thermal dissipation for RF amplification on board of spacecraft. Intense R&D efforts are ongoing worldwide, strengthened by the GaN semiconductor technology, to ever increasing switching frequencies, voltage levels and power levels, and the technique is soon going to be within the reach of space applications. ESA has started its own R&D investigation on the subject many years ago, with TRL 3 for the whole ET system to be reached by 2017. By then, Industry is expected to be ready to bring the maturity level from TRL3 up to TRL5 by developing, manufacturing and testing an EM of the ET system.

6. ACKNOWLEDGEMENT

TAS Belgium is greatly acknowledged for its contribution to the funding of the NPI activities covered by the present paper.

7. REFERENCES

1. "Performance and Simplicity in Power Conversion Functions Made Possible by New European Components", F. Tonicello, O. El Korashy, A. Pesce, 9th European Space Power Conference, Saint-Raphael, France, 6-10 June 2011

2. "High Efficient Universal Buck Boost Solar Array Regulator SAR Module", S. Kimmelmann, W. Knorr, 10th European Space Power Conference, Noordwijkerhout, The Netherlands, 13-17 April 2014

3. "Generation 4 eGan FETs Widening the Performance Gap with the Aging MOSFET", A. Widow, Efficient Power Corporation, EEWeb, 28 October 2014

4. "GaN FET module performance advantage over silicon", N. Mehta, Texas Instrument, March 2015

5. "A 90% Efficient 50 MHz Buck Converter for Space Telecom Systems", F. Leroy, O. Deblecker, F. Dualibe, N. Le Gallou, C. Delepaut, 10th European Space Power Conference, Noordwijkerhout, The Netherlands, 13-17 April 2014

6. "Over 10 MHz Bandwidth Envelope-Tracking DC/DC Converter for Flexible High Power GaN Amplifiers", N. Le Gallou, D. Sardin, C. Delepaut, M. Campovecchio and S. Rochette, IEEE MTT-S International Microwave Symposium, Baltimore, USA, 5-10 June 2011

7. "Radio-Frequency High Power Amplifier with Broadband Envelope Tracking by Means of Reversed Buck Converter", ESA patent, publication numbers: WO2014170710, US 2016/0056770

8. "A 15 W L-Band Floating-Supply GaN RF PA for Envelope Tracking Systems in Space Applications", T. Kuremyr, C. Delepaut, N. Ayllon, Wolfgang Heinrich, O. Bengtsson, to be submitted for publication to IEEE Transactions on Microwave Theory and Techniques