Influence of Parasitic Inductances on Switching Performance of SiC MOSFET

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Abstract. Compared to the silicon power devices, silicon carbide device has shorter switch time. Hence, as a result of the faster transition of voltage (dv/dt) and current (di/dt) in SiC MOSFET, the influence of parasitic parameters on SiC MOSFET's switching transient is more serious. This paper gives an experimental study of the influence of parasitic inductance on SiC MOSFET's switching characteristics. Most significance parameters are the parasitic inductances of gate driver loop and power switching loop. These include the SiC MOSFET package's parasitic inductance, interconnect inductance and the parasitic inductance of dc link PCB trace. This paper therefore focuses on analysis and comparison of different parasitic parameters under various operation conditions in terms of their effect on overvoltage, overcurrent and switching power loss.

1 Introduction

Power semiconductor devices are attracting increasing attention as key components in a variety of power electronic systems. Silicon power devices have improved significantly over the past several decades, but they are now approaching performance limits imposed by the fundamental material properties of silicon, and further progress can only be made by migrating to more robust semiconductors [1]. As a wide-bandgap semiconductor, Silicon carbide device has superior physical and electrical properties such as the high blocking voltage, high-frequency capability, high-temperature tolerance and low-loss.

An increase in switching frequency has always been in great quest to push up the power density and facilitate the miniaturization of power electronics converters [2]. Due to SiC MOSFET's fast switching speed, it is gradually obtaining the widespread application in high-frequency power converters. However, in the traditional hard switching converter topology, high speed silicon carbide MOSFET device results in a very fast switching transient thereby subjecting the converter to bear higher du/dt and di/dt. The larger slopes of the voltage and current will induce larger current and voltage respectively in stray capacitances and inductance in the converter circuit. This leads to larger overshoots in voltage and current profiles with the potential effect of damaging SiC MOSFET device. In addition, electromagnetic oscillation may also occur due to the interaction between the voltage and current transitions with the circuit stray inductance and capacitance. This may increase switch losses as well as contributing to electromagnetic interference problems.

There has been a significant effort on the study of SiC MOSFET, but the majority of research have focused on the design, packaging, modeling and application of SiC MOSFET power device [3-6]. Only a few studies on the influence of parasitic parameters on SiC power MOSFET switching characteristics have been mentioned. Investigations into the effect of parasitic elements on switching performance of power device can be classified into three categories. The first method focuses on the extraction and modeling of these parasitic parameters with ANSYS Q3D to measure their effect using circuit simulations [7-8]. This, however, needs a precise device model. The second method involves developing an analytical model of the MOSFET [9-11]. But it is very difficult to obtain the accurate analytical expressions of the whole switching transient characterization in case of taking account of all parasitic elements. Therefore, certain parasitic elements such as gate inductance and the change of terminal parasitic capacitance of MOSFET may be neglected. The last approach is the experimental method. Though the method still cannot suffice to explain the physical meaning behind those observations, it can intuitively display the relationship between parasitic parameters and switching performance, and show the level of influence of each parasitic parameter [12-13].

This paper analyzes circuit operation and

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systematically studies the effects of individual parasitic inductance under various operation conditions by conducting lots of experiments. All the gate loop and power switching loop parameters have been independently controlled and studied based on the SiC MOSFET switching characterization test bench. Their influences on SiC MOSFET switching characteristics can be shown from the experimental waveforms. Moreover, the degree of influence of all parameters have been evaluated in terms of overvoltage, overcurrent and switching loss.

2 Test Circuit Operation Simply Analysis

Most of the power electric systems usually operate under clamped inductive load, and the load inductance is relatively large. After SiC MOSFET switches off, the load inductance current generally will not be discontinuous as it continues flowing through the freewheeling diode. When SiC MOSFET turns on, there will be a diode reverse recovery process. The single pulse experiments cannot reflect the diode reverse recovery process. Hence, a double pulse test (DPT) has been used for evaluating SiC MOSFET's switching characteristics in this work. Double pulse test schematic is shown in Fig. 1. The gate driver test signal is a double pulse waveform as shown in Fig. 2.

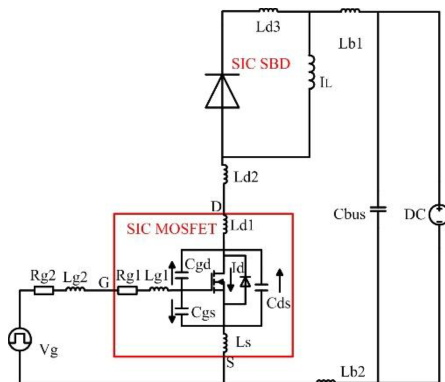


Fig.1 Double pulse test equivalent circuit with parasitic parameters

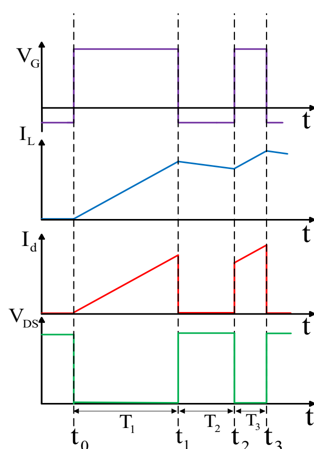


Fig.2 Double pulse test waveforms

At time t_0, the SiC MOSFET which is the device under test (DUT) is turned on. It is held on until current reaches the desired level. At time t_1, the gate is forced to negative level and the turn-off switching characteristics of the SiC MOSFET and the turn-on characteristics of the diode are recorded. During t_1-t_2, the SiC MOSFET is kept off and the inductor current freewheels through the diode. At time t_2, the device is turned back on. The turn-on characteristics of SiC MOSFET and the turn-off characteristics of the diode are then captured. At time t_3, the SiC MOSFET is turned off, the measurement is completed and then the inductor current falls to zero through the freewheeling diode.

The schematic of this circuit taking consideration of all parasitic parameter is shown in Fig. 1. Based on derivation of Faraday's Law, it is clear that inductance is only defined for a closed contour. According to the loop concept, for the stray inductances' parameters to be studied, the network's stray inductance can be narrowed down to three primary lumped inductances according to the current paths. 1) the gate loop inductance, L_G, formed by the gate current path, where $L_g= L_{g1}+L_{g2}$; 2) the main switching loop inductance, L_d, formed by the drain current path, which includes the stray inductances of the MOSFET and Diode packages as well as PCB interconnections, $L_d=L_{d1}+L_{d2}+L_{d3}+L_{b1}+L_{b2}$; 3) the common source inductance L_S that exists in both loops, which can be treated as a mutual inductance between the gate loop and the switching loop.

3 Experimental Study Of The Parasitic Parameters

3.1 Hardware setup

In order to evaluate the parasitic parameters impact on the device switching performance, the DPT bench needs to be designed and optimized. The implemented prototype is designed to accommodate a TO-247 for the switch and the diode. The test circuit is constructed using a 1200V/36A SiC MOSFET C2M0080120D and a 1200V/33A SiC Schottky diode C4D20120D from Cree Semiconductor in TO-247 package. As shown in Fig.3, the test platform includes 4 parts of PCB including the digital signal processor (DSP) evaluation board 00IC TOP2812, gate drive board, isolation type power supply board and dc bus board. The DSP system board is used to generate the required double pulse control signal. The gate drive board uses the ACPL-W343 driver chip which is internally integrated with an optical coupling isolation to magnify the control signal. At the same time, the isolation type power supply board based on MORNSUN QA01C is used to provide positive and negative bias voltage for gate driver. In addition, a + 24 V and -5 V transient suppression diodes are connected between the gate and source terminals to protect gate from breakdown.

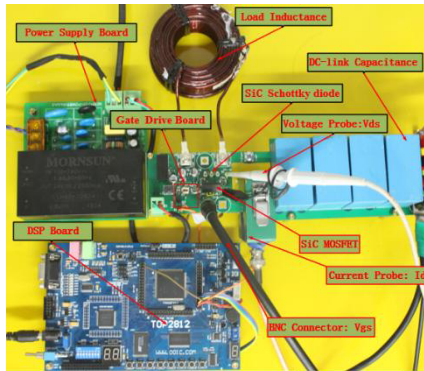


Fig.3. Double pulse test bench

3.2 Analysis of switching characteristics

Due to the parasitic inductances and a di/dt during switching time, there are inductive voltage drops or overshoot across the parasitic inductances. These voltages together cause a voltage drop on the drain-source voltage:

$$\Delta V_1 \approx L_{\text{loop}} \frac{\mathrm{d}i_{\text{f}}}{\mathrm{d}t} \tag{1}$$

$$\Delta V_2 \approx L_{\text{loop}} \frac{\mathrm{d}i_{\text{r}}}{\mathrm{d}t} \tag{2}$$

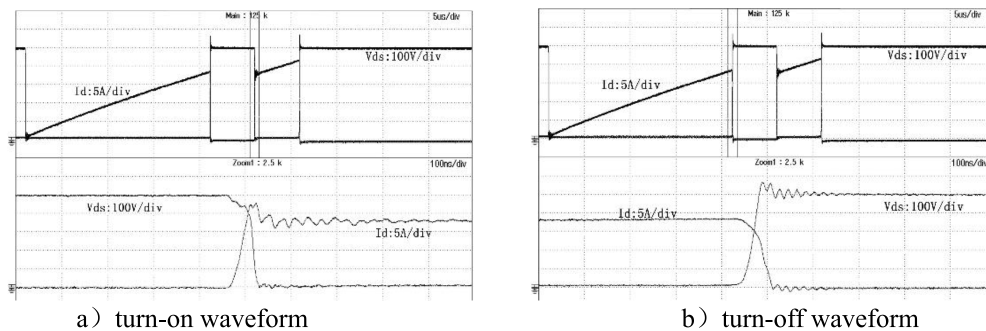
Where:

$$L_{\text{loop}} = L_{\text{d}} + L_{\text{s}} \tag{3}$$

The MOSFET switching waveforms under the influence of this inductance is shown in Fig. 4. The device is switched under 500 V and 18 A condition with a gate resistance R_{G} of 37 Ω. In the experiment, total power loop parasitic inductances of the test bench are estimated and compared by Eq.1 and Eq.2 in table I. The result shows that the average of total power loop parasitic inductances is about 136nH.

Table 1. Total Power Loop Parasitic Inductance Computation

Compute by Eq.1			Compute by Eq.2		
ΔV_2	$\mathrm{d}i_{\text{r}}/\mathrm{d}t$	L_{loop}	ΔV_1	$\mathrm{d}i_{\text{f}}/\mathrm{d}t$	L_{loop}
60V	434A/μs	138nH	56V	418 A/μs	134nH



a） turn-on waveform b） turn-off waveform

Fig.4. Experimental drain current and drain-source voltage waveforms

3.3 Influence study of different parasitic inductances

To study the influence of these parasitic parameters, the current paths in the tester have been broken at several points, in which way small different inductances can be inserted into the loop to mimic the change of parasitic ones. The different inductances are made of several air-core coils with the corresponding inductances of 20nH, 34nH, 48nH, 64nH, and 77nH. In the experiment, each type of stray parameter is controlled with the rest of the parameters kept constant, such that its effect can be studied independently. The influence on the device stress is shown in Fig. 5, which indicate that the gate loop parasitic inductance has only a minor effect on the SiC MOSFET switching waveforms. The drain-source voltage overshoot increases with the increase of power loop parasitic inductance L_{d}. Compared to the voltage overshoot without insertion of an additional inductor, the voltage overshoot with insertion of a 77nH inductor increases by approximately 8%. However, drain current overshoot decreases with the increase of inductance L_{d}. The common source inductance L_{s} relieves the device of switching stresses by slowing down the switching process due to its negative feedback nature. Due to the fast switching characteristic of SiC devices, the change rate of voltage and current is faster than Si devices. The same L_{d} with a lager current rate will result in larger voltage overshoot, similarly, L_{s} will cause the slower switching speed. So L_{d} and L_{s} have a greater impact on the switching process of SiC than Si devices. In addition, Fig.6 shows the effect of parasitic inductances on the switching energy E_{on}, E_{off} and E_{total}. According to IEC standard, they are defined as follows.

$$E = \int_{t_1}^{t_2} V_{\text{ds}} \cdot I_{\text{d}} \mathrm{d}t \tag{4}$$

$$E_{\text{total}} = E_{\text{on}} + E_{\text{off}} \tag{5}$$

As is shown in Fig.6, the increase in L_{g} almost did not affect the switching energy. L_{d} reduces the turn-on energy a little bit due to its snubber effect, and increases

the turn-off energy a little bit due to the higher V_{ds} overshoot. However, the total loss of both L_g and L_d are still almost unchanged. Fig.6 also indicate that L_s has more influence on switching energy. The switching energy at turn-on and turn-off transients significantly increases with greater L_s. This is because the inductance L_s forms negative feedback in gate drive loop, and increases the switching time. The total switching loss when an additional 77nH inductance is inserted is approximately three times bigger than E_{total} without insertion of the inductance. For Si devices, larger L_s will also leads to increased switching loss, but the effect is relatively small.

3.4 Influence of parasitic inductances under different load current

Fig.7 shows the influence of parasitic inductances on voltage overshoot and current overshoot under different values of load current. The experimental bus voltage is kept constant at 500V. It is observed that the relationship between voltage overshoot and load current is almost linear, which proves the correctness of the Eq.1. On the basis of the rated current, the current overshoot percentage increases a little bit due to the increase of slope of current with greater load current.

3.5 Influence of parasitic inductances under different bus Voltage

In the practical application, the device maybe work under different voltage levels. In order to estimate the influence of parasitic parameter on SiC MOSFET electrical stress, many experiments are conducted in this paper under a variety of bus voltages. As shown in Fig.8, the drain-source voltage overshoot almost remains constant, which implies that the overshoot is not dependent on the bus voltage level. However, for the higher voltage levels, the overshoot is relatively smaller. Due to the constant length of the switching period, the higher the bus voltage the greater the slope of drain-source voltage. Hence, the voltage transition would induce a displacement current on the output capacitance of the device, thereby increasing the current overshoot in turn-on transient.

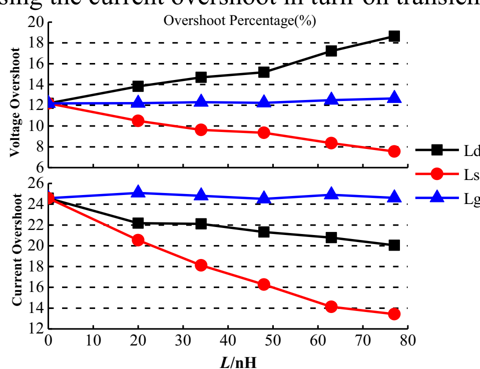


Fig.5. SiC MOSFET stress vs. various parasitic inductance

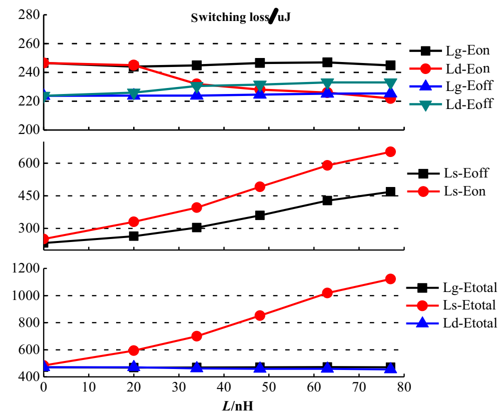


Fig.6. SiC MOSFET switch loss vs. various parasitic inductance

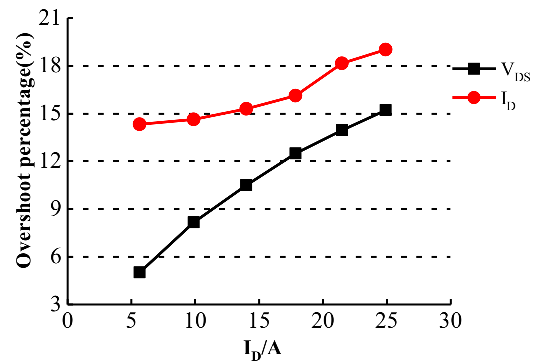


Fig.7. SiC MOSFET stress under load current

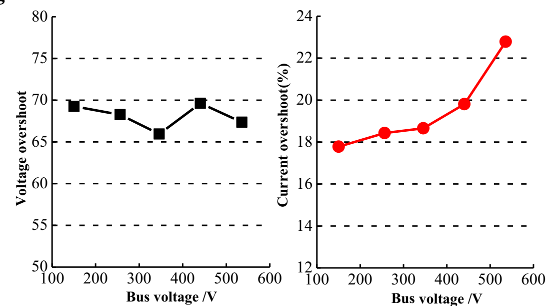


Fig.8. SiC MOSFET stress under various bus voltage

4 Conclusion

This paper has systematically studied the influence of the parasitic inductances under various operating conditions on the SiC MOSFET's switching characteristics, electrical stress and switching loss. It is shown that a larger power loop inductance will result in more voltage overshoot but less current overshoot. The larger inductance will also lead to more turn-off losses but less turn-on losses while the total loss remains unchanged. It's found that the common source inductance has the most significant effect on the switching performance because it is included not only in the main power circuit but also in the gate drive circuit. The experimental results show that the inductance, Ls, slows down the turn-on and turn-off processes, thus increasing the turn-on and turn-off switching power losses. The conclusion is useful for switching loss measurement system design, and the

common source inductance should be minimized for realizing a good switching performance.

Acknowledgement

This work was supported by the National Key Research and Development Program (2016YFE0102800)

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