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Electric Field Analysis of Press-Pack IGBTs

XinlingTang[1], *Yan* Pan[1], *Yanfang* Chen[1], *Pengyu* Fu[2] and *Zhibin* Zhao[2]

[1]State Key Laboratory of Advanced Power Transmission Technology (Global Energy Interconnection Research Institute of State Grid Corporation of China), Beijing 102209, China
[2]State Key Laboratory of Alternate Electric Power System with Renewable Energy Sources (North China Electric Power University), Beijing 102206, China

Abstract. High voltage IGBT module is the ideal option for the VSC-HVDC power transmission application. At present, wire-bonded technology and press-pack technology are available packaging technologies for high voltage IGBT. The press-pack IGBTs have such advantages as low inductance, low thermal impedance and short circuit failure mode than the wire-bonded IGBT module, which especially suit for high voltage power transmission application by series connection. However, the electrical insulation failure modes of press-pack IGBTs are much less known with limited literature published. In this paper, we presented the electric field analysis of a 3D press-pack IGBT model under DC rating voltage test condition. The electric field distribution of the press-pack IGBT stack was solved as an electrostatic problem by employing the finite element method. The results revealed the potential electrical insulation failure modes of the press-pack IGBTs: corona discharge at the edge of silver plate, partial discharge at the micro gap between die and PEEK frame and creeping discharge at the surface of PEEK frame.

1 Introduction

The demand to achieve a balance between environment and energy is urgent. The fossil energy supports the industrialization of human society but also causes the greenhouse effect. Searching for clean and renewable energy alternatives is key importance to the development of human society. However, the bulk distribution of available alternatives (such as wind, solar etc.) is usually far from the load center (especially in China). Achieving bulk and reliable transmission of the clean and renewable energy is a technological challenge.

HVDC power transmission technology is a key technology to realize the integration of clean and renewable energy to the power grid [1]. Power electronics is an enable technology to achieve the conversion and control of power. Power electronics based converter is the key component of HVDC power transmission system. In fact, HVDC power transmission technology is mainly subdivided into two categories: LCC-HVDC and VSC-HVDC according to the power semiconductor devices used in the converter. The half-controlled thyristors are used in the converters of LCC-HVDC technology. However, the full-controlled devices (such as IGBT, IEGT) are used in the converters of VSC-HVDC technology. Comparing with LCC-HVDC technology, VSC-HVDC technology is more flexible and is especially suitable for integrating the versatile renewable energy into the power grid.

Continuous improvements in the device design and in their manufacturing process have gradually increased the ratings of the IGBT. The VSC-HVDC converter is a main application of the high voltage and high power IGBT device. In the power transmission application, a high level of reliability of the device is required to prevent costly or catastrophic failure. In this context, the device packaging is assumed to play a critical role. At present two packaging technologies for IGBT devices are available for application in the MW power range: the wire-bonded IGBT module and press-pack IGBTs. Power modules have been object of extensive investigation including their characterization under variable operating conditions and the analysis of failure mechanisms [2]. The press-pack packaging eliminates bonding wires and solder layers, and is claimed to offer improved reliability [3]-[5]. However, the knowledge on press-pack IGBTs is much less mature with only limited literature published. In addition, High voltage blocking capability is one of the most important performance for the press-pack IGBTs. Therefore, the analysis of the electrical insulation failure modes of press-pack IGBTs needs to be performed.

2 Insulation Failure of Press-Pack IGBT

In Fig.1, the explosive view and schematic of the cross section of a conceptional press-pack IGBTs are shown. The packaging technology evolves from press-pack thyristors and GTOs, which have proven to be excellent in ruggedness and reliability [2]. Press-pack thyristors and

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GTOs use a single large die in the capsule. However, it is still not feasible to fabricate a single large IGBT die for high voltage application from a single wafer due to the fine pattern of the IGBT cell structure. To overcome the technological challenge, press-pack IGBT is developed as a multi-die device, as shown in Fig. 1. The device consists of multiple die stacks, and each stack is composed of an IGBT or FRD die, two molybdenum plates, and a die frame. The emitter electrode is multi-stamp and collector electrode is single-stamp. Both electrodes transfer the external clamping force to the individual IGBT or FRD stack.

High operating voltage (⩾3300V) of IGBT device results in higher demands on electrical insulation capability as well as partial discharge resistance [6]. Unlike the power module in which silicone gel is used to provide the dielectric strength necessary to guarantee the required insulation capability [7], [8], press-pack IGBT uses protective gas to provide electrical insulation. When studying the insulation failure mechanism of high voltage press-pack IGBT, the dies, the protective gas and the plastic die frame should be the main concerns.

In the press-pack IGBTs, the main insulation aging processes are partial discharge and creeping discharge. Partial discharge occurs in the protective gas when the electric field exceeds the critical electric field, which depends on the pressure and the gas gap. Creeping discharge occurs at the interface of gas and dielectric when the tangent electric field exceeds the critical electric field, which depends on the dielectrics and the condition of the gas. To improve the electrical insulation performance of press-pack IGBTs, it is essential to analyze the electric field distribution in the structure.

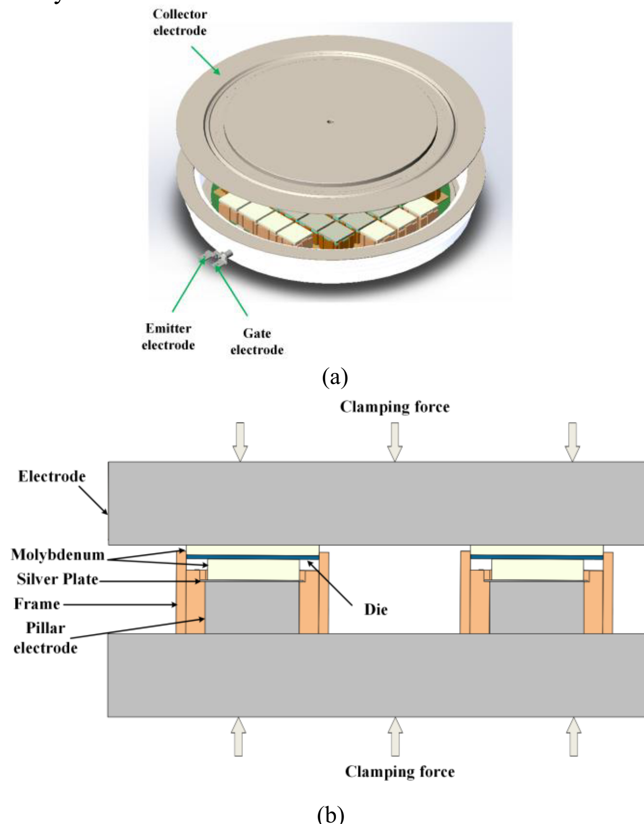

Fig. 1. Press-pack IGBTs. (a) explosive view. (b) Schematic of its cross section view

3 Electric Field Simulation

3.1 Modelling of a Press-Pack IGBT Stack

Press-pack IGBT is a mulit-die device. When analyzing the electric field of the press-pack IGBT under rating voltage test, it only needs to analyze the electric field of a single IGBT stack. In Fig. 2, a 3-D model for the analysis of a press-pack IGBT stack is presented. In the model, the IGBT stack is located in the center of the solving region. The outer box is the equivalence of the package housing. The upper surface is an analogy to the collector side and the lower surface is an analogy to the emitter side. The other 4 surfaces are an analogy to the ceramics of the package housing.

The model simulates the condition of press-pack IGBTs under V_{CES} type test [9]. The V_{CES} (3300V) is applied to the collector of IGBT die, the molybdenum plate attached to the collector of the IGBT die, and the collector side of the outer box. Zero voltage is applied to the emitter of the IGBT die, the silver plate, the molybdenum plate attached to the emitter of the IGBT die and the emitter side of the outer box. The other 4 surfaces are set to be Neumann boundary condition of the electric potential.

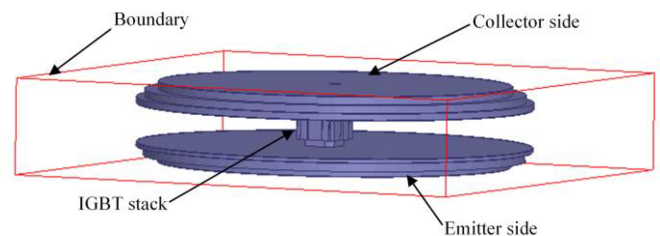

Fig. 2. 3-D model for the analysis of a press-pack IGBT stack

3.2 Analysis Method

The fundamental description of all macroscopic electromagnetic phenomenon is Maxwell equations:

$$\begin{cases} \nabla \cdot \vec{\boldsymbol{D}} = \rho \\ \nabla \times \vec{\boldsymbol{E}} = -\dfrac{\partial \vec{\boldsymbol{B}}}{\partial t} \\ \nabla \cdot \vec{\boldsymbol{B}} = 0 \\ \nabla \times \vec{\boldsymbol{H}} = \vec{\boldsymbol{J}} + \dfrac{\partial \vec{\boldsymbol{D}}}{\partial t} \end{cases} . \quad (1)$$

When the rate of change of the system is low, the electric filed induced by the changing magnetic field could be neglected. If the electric field of the system only has Coulomb field component, then this kind of electric field is called quasi-static electric field. In this context, the electric field of the press-pack IGBT stack could be assumed to be quasi-static electric field due to the low change rate of magnetic field. Under this assumption, the electric field could be represented as

$$\vec{\boldsymbol{E}} = -\nabla \varphi . \quad (2)$$

In equation (2), φ represents the electric potential. Do the divergence operation to the both side of the fourth equation in (1), and we obtain

$$\nabla\cdot(\nabla\times\boldsymbol{H})=\nabla\cdot(\vec{\boldsymbol{J}}+\frac{\partial\vec{\boldsymbol{D}}}{\partial t})=0 \quad (3)$$

Substituting $\vec{\boldsymbol{J}}$ and $\vec{\boldsymbol{D}}$ in (3) with $\vec{\boldsymbol{J}}=\gamma\vec{\boldsymbol{E}}$, $\vec{\boldsymbol{D}}=\varepsilon\vec{\boldsymbol{E}}$ and $\vec{E}=-\nabla\varphi$, the equation (3) is changed into

$$\nabla\cdot(\gamma\nabla\varphi)+\nabla\cdot(\frac{\partial}{\partial t}(\varepsilon\nabla\varphi))=0 \ . \quad (4)$$

The phasor form of equation (4) is

$$\nabla\cdot(\gamma\nabla\dot{\varphi}+j\omega\varepsilon\nabla\dot{\varphi})=\dot{0} \ . \quad (5)$$

In equation (5), $\left|\dot{\boldsymbol{J}}_{\mathrm{c}}\right|=\left|\gamma\nabla\dot{\varphi}\right|$ represents the conduction current and $\left|\dot{\boldsymbol{J}}_{\mathrm{d}}\right|=\left|j\omega\varepsilon\nabla\dot{\varphi}\right|$ represents the displacement current.

When deciding the electric field control equation of a region filled with material, the electric property of the material is vital. The ratio of $\left|\dot{\boldsymbol{J}}_{\mathrm{d}}\right|$ to $\left|\dot{\boldsymbol{J}}_{\mathrm{c}}\right|$ is

$$\frac{\left|\dot{\boldsymbol{J}}_{\mathrm{d}}\right|}{\left|\dot{\boldsymbol{J}}_{\mathrm{c}}\right|}=\frac{\left|j\omega\varepsilon\nabla\dot{\varphi}\right|}{\left|\gamma\nabla\dot{\varphi}\right|}=\frac{\omega\varepsilon}{\gamma} \quad (6)$$

If the ratio is much smaller than 1, the electric field of the region could be assumed to be controlled by electrostatic field. Otherwise, if the ratio is much larger than 1, the electric field of the region could be assumed to be controlled by DC electric field. The two electric field types mentioned above are constant. Equation (4) descripts the time-varying process of electric field. From Equation (4), the transition process of the electric field can be characterized by the relaxation time

$$\tau_{\mathrm{r}}=\frac{\varepsilon}{\gamma} \quad (7)$$

If the test duration is much shorter than the relaxation time, then the electric field should be analyzed by using the electrostatic field. Otherwise, DC electric field should be used.

The electric property of important materials involved in the model is shown in Table I [10]-[11]. The relaxation time of metals in the model is much lower than 1s, and the metals are considered to be electrostatic. The relaxation time of PEEK is 47.2 min, and the relaxation time of N_2 is 24.6 h. During the short DC test, the test time is much lower than the relaxation time of dielectric materials. Therefore, the electric field distribution is governed by electrostatic field. Under the power frequency voltage test, the ratio of $\left|\dot{\boldsymbol{J}}_{\mathrm{d}}\right|$ to $\left|\dot{\boldsymbol{J}}_{\mathrm{c}}\right|$ of the dielectric material region is much higher than 1. Therefore, the electric field distribution is governed by electrostatic field.

Table 1 Electric parameters of dielectric materials in the model

Material	Electric conductivity γ ($\Omega\cdot$m) (25°C)	Relative dielectric constant ε_r
PEEK	10^{-14}	3.2
N_2	10^{-16}	1.00058

The analysis is solved by employing Finite Element Method (FEM). However, the typical electromagnetic field solver does not solve the semiconductor equations. Many TCAD softwares are developed to fulfill this purpose (such as Silvaco). But for electric field analysis in the package, they are complex to use. In this simulation, IGBT die is modelled as silicon, and the dielectric constant of silicon was employed. The surface exception the one including emitter of the die is set to be 3300 V. This assumption is an ideal behavior for the IGBT die. In fact, due to the development of the die edge termination technique (such as guard rings or Junction Termination Extension), the manufacture of the die is toward to this goal. But the local electric field enhancement should be concerned, it could result in the partial discharge in the protective gas on the passivation layers of the IGBT dies. This situation is complex and is not considered in the simulation.

4 Results

The model of a press-pack IGBT stack is solved as an electrostatic problem by using the finite element method. Fig. 3 shows the electric potential lines around the metals and dies. The electric potential lines around the metallization edge of the die emitter and the silver plate are highly uneven distributed. The electric field at these regions could be highly reinforced, therefore weaken the electrical insulation of the device. The reinforcement of the electric field on the surface of die should be considered during the die design process.

Various edge termination techniques and passivation layers should be adopted to avoid the occurrence of partial discharge on the die surface under the rating voltage test. If the edge termination and passivation of the chip is good enough to block the rating voltage, then the chip surface should not be the weak point in this packaging structure. Another weak area is the edge of the silver plate. Comparing with other metals used in the structure, the silver plate is much thinner and has a relatively sharper corner. The analysis result in Fig. 3 shows that the electric potential lines are condense around the corner of the silver plate. It is highly risky to occur corona discharge at the corner of silver plate in the protective gas.

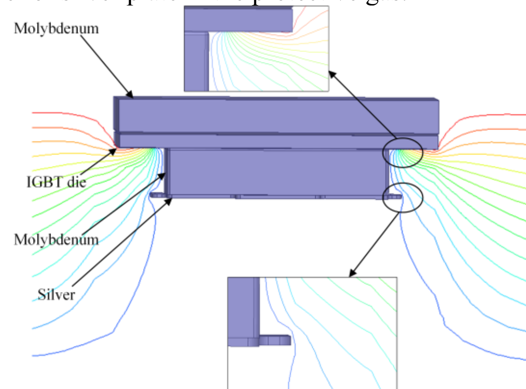

Fig. 3. Electric potential lines around the metals and dies

On the other hand, the creeping discharge of dielectric material should be considered. Fig. 4 shows the electric potential distribution in the PEEK frame. The upper branch of the PEEK frame has a dramatic voltage drop, and the tangent component of the electric field is high. As the trace P1 to P2 shown in Fig. 4, it is possible to occur creeping discharge at the surface of the PEEK frame. Another region should be considered is the micro gap between the chip and PEEK. If the gap between the chip and PEEK is too narrow, the potential difference between the two may be high enough to cause micro-arcing in the gap. In this model, the gap between the PEEK and chip is wide enough to avoid this failure mode.

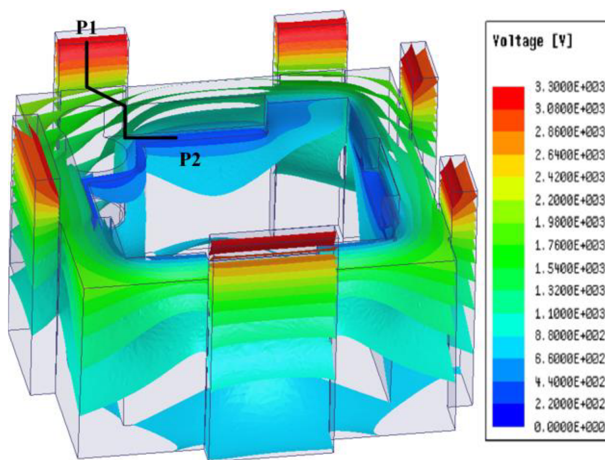

Fig. 4. Electric potential distribution in the PEEK frame

Fig. 5 shows the electric field distribution of the PEEK frame and the surface of the silver plate. The maximum electric field intensity is 9.16 kV/mm, which is located at the corner of the silver plate. The dielectric strength of the nitrogen gas is 3.3 kV/mm at 25°C and 1 atm[11]. The maximum electric field intensity on the silver plate is far beyond the dielectric strength and the corona discharge at the corner of the silver plate is expected. The result of electric field analysis shows that the die surface has a maximum field strength of 85 kV/mm. However, this unexpected high value is caused by the assumption made during the modelling. In fact, the die used in the device passes the rating voltage test for the bare die. The edge termination and passivation of the chip should be well-designed to avoid the breakdown on the surface of die. The electric field analysis result about the die could be taken as a reference, but the electric field analysis results about the other components are reliable.

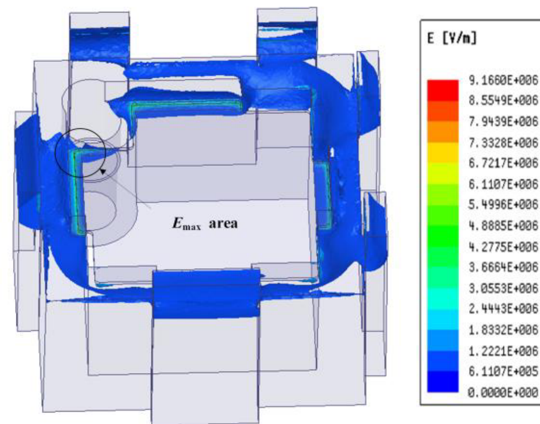

Fig. 5. Electric field distribution of PEEK frame and silver plate

5 Conclusions and Outlook

The electric field analysis of a press-pack IGBT stack was performed by using an FEM based electromagnetic field solver. The electric potential distribution and the electric field intensity were calculated during the V_{CES} test condition for the press-pack IGBTs. During the analysis process, we mainly concern three kinds of insulation failure modes: corona discharge, partial discharge and creeping discharge. For the present packaging structure, the calculation results show that:

1) The maximum electric field intensity at the edge of the silver plate is much higher than the electric strength of the protective gas N_2. It is highly risky to occur corona discharge at this region.

2) The chip region is an electrical insulation weak point of the assembly. The potential partial discharge at the surface of the chip should be considered during the chip design process. The chip used in the device should firstly pass the rating voltage test for the bare die. The micro gap between the chip and PEEK frame should be avoid to occur the micro-arcing at this region.

3) The potential creeping discharge at the surface of PEEK should be concerned. The tangent component of the electric field at the PEEK surface may be high enough to result in the creeping discharge.

The analysis presented in the paper shows the potential electrical insulation failure mode of the device under the rating voltage test. Further experiments should be done to verify the conclusions made here. The partial discharge characteristics of the protective gas and the creeping discharge characteristics of the insulation material in the protective gas should be investigated in these experiments. Another work should be done is to study the electrical insulation failure modes of the devices under other test conditions (such as reliability test).

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