Power Distribution Design of MicroSat Power Control Unit Elegant Bread Board (EBB)

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Abstract. The Power Control Unit (PCU) in Micro-satellites program proposed to develop by NSPO, acts as the satellite power control and distribution center. One of the modules in the PCU, named the Power Distribution (PD), the main function provides the rated voltage and current of each power outlet for the satellite subsystem. When overload or short-circuit happens and persists for a time period, PD will limit the load current in a pre-designed value, and shut off the load to avoid damage on essential devices. In this paper, we will introduce the PCU EBB function and circuit design of PD.

1 Introduction

"Microsat" is usually applied to the name of an artificial satellite with a wet mass between 10 and 100 kg (22 and 220 lb). [1] However, this is not an official convention and sometimes those terms can refer to satellites larger than that, or smaller than that (e.g., 1–50 kg (2.2–110.2 lb)).

MicroSats can be built smaller than regulator satellites to reduce the large economic cost of launch vehicles and the costs associated with construction. Miniature satellites, especially in large numbers, may be more useful than fewer, larger ones for some purposes – for example, gathering of scientific data and radio relay. Technical challenges in the construction of MicroSats may include the lack of sufficient power storage or of room for a propulsion system.

Aimed at building a sustainable space industry, National Space Organization (NSPO) proposes to develop Micro-satellites program. The major goal for this program is to cooperate with domestic academia and industry developing the space components, subsystems, system, and forming space. This paper will focus on Power Control Unit architecture description for MicroSat satellite and the Power Distribution circuit design in the PCU Elegant Breadboard (EBB).

2 Power control unit

The Power Control Unit (PCU) in MicroSat is similar to a human heart. PCU is in charge of receiving solar power from solar arrays and regulating battery charging current according to On Board Computer (OBC) commands. It also controls and distributes power to various satellite load users upon the request of OBC command. A PCU block diagram is shown in Fig. 1.

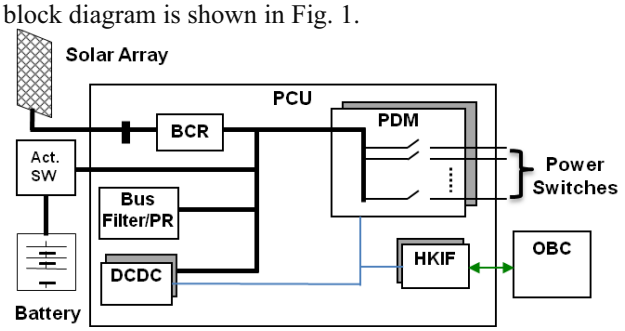

Fig. 1. Function Diagram of Power Control Unit

The PCU consists of 5 main functions, i.e. Power Distribution, Battery Charge Regulation, DC-DC Conversion, Power Relay, and Housekeeping Interface. Their main functions are as following:

- Convert input solar power to spacecraft required power by means of executing pulse width modulation switching commands received from OBC
- Provide Battery over voltage hardware protection
- Distribution of unregulated primary electrical power via over-current protected outlets to bus and instrument units as well as electrical heaters upon OBC command
- Distribution of thermostatic-control heater Activation of solar array Hold Down& Release Mechanism (HDRM) upon OBC command

• Activation of propulsion equipment upon OBC command
• Hardware protection of spacecraft main bus power under-voltage and preserve recovery capability
• Manage OBC main processor initialization and failure detection, recovery
• Provision of status monitoring and tele-command interfaces allowing the system and ground operate the power system, evaluate its performance and initiate appropriate countermeasures in case of abnormal conditions

3 Power distribution module

The Power Distribution (PD) in the PCU EBB provides the rated (MainBus) voltage and current of each power outlet for the satellite unit. MainBus voltage is the tie point for power from the solar arrays and the Battery [2]. Each power outlet for the satellite unit is controlled by power switches. The PDM contains 66x power switches of which 58 power outlets are available. For each power outlet, the power switches are implemented with power MOSFETs, and executed ON/OFF control by the FPGAs [3].

3.1 Architecture

According to sub-system requirements, The PD is separated from several outlet architectures. Some power outlets only have one switch; some outlets are configured in series for loads or with parallel outputs for special units. Architecture of Power Distribution module is shown in Figure 2.

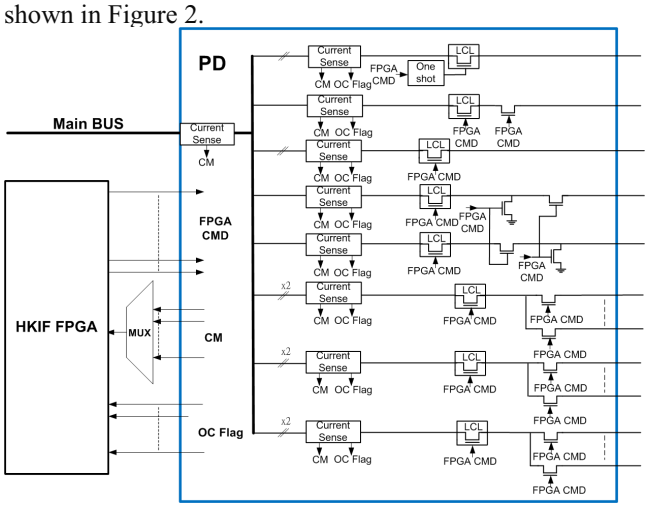

Fig. 2. Architecture of Power Distribution module

3.2 Circuit design

Whatever the sub-system voltage and load current requirements are, The PD outlets have the same functionality and similar circuit design, as shown in Figure3. Each power outlet both includes a power switch control circuit, current sensing circuit, the transistor feedback circuit, over current detector and current monitor. For convenient design, there are three level outlets in PDM.

Table 1. List of Outlet Types

#	Switch/Current Monitor	Current Monitor Range	Max Load		Latch Current Limitation	Trip-off current	Trip-off time
			Max Power	Current			
A	+	5.00A	50W	2.27A	6.82A	3.41A	5ms
B	+	5.00A	110W	5A	-	7.50A	5ms
C	+	1.00A	20W	0.91A	2.73A	1.36A	5ms

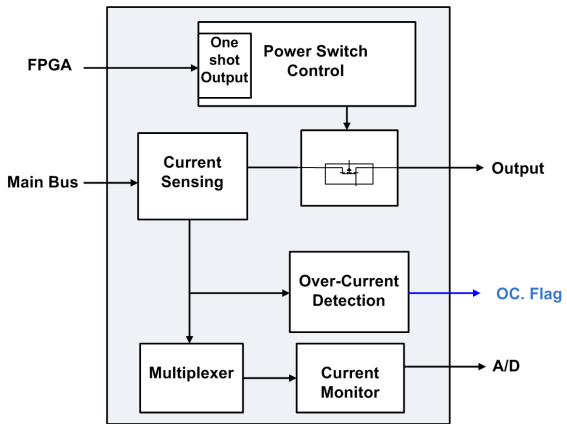

Fig. 3. Power Distribution function

3.3 Power switch control circuit

In PD module system, power switch control circuit is designed to on/off control the power output to the load. This circuit is controlled by FPGA to turn on/off the power MOSFET switch. In order to meet the requirements, the choosing of the power MOSFET should consider the characteristics of absolute maximum voltage and drain current rating, as well as on/off response time, and rise/falling time. Its design circuit is shown in Figure 4.

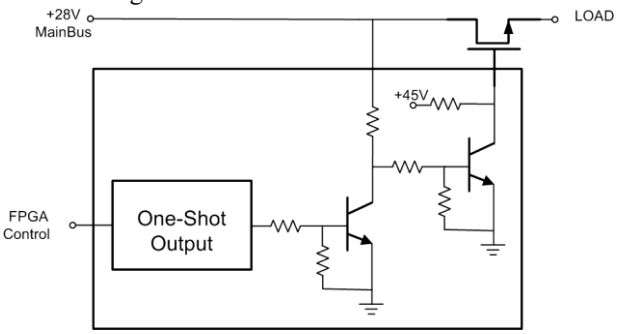

Fig. 4. Power switch control circuit

Without redundancy design in PCU EBB, when an over current occurred by OBC / S-band receiver, the protection process will power cycle OBC / S-band receiver by using a one-shot output which provide one second pulse to turn off and on again OBC / S-band receiver.

The one-shot output circuit is implemented with a mono-stable multi-vibrator featuring both positive and negative edge trigger inputs which can be used an inhibit input Complementary output pulse is provided.

There are three trigger inputs from the device. Inputs (A) are active-low trigger transition inputs and input (B) is an active-high transition Schmitt-trigger input. For OBC / S-band receiver protection, inputs (A) are fit in with our purpose to power cycle load.

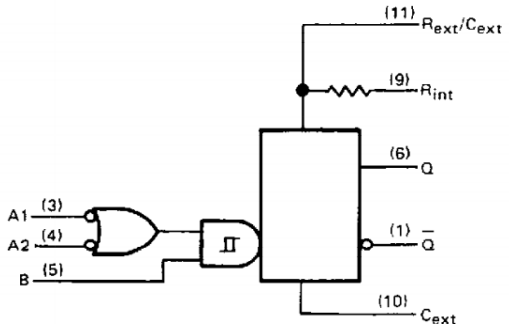

Fig. 5.one-shot output circuit

An internal timing resistor is provided for design convenience minimizing component count and lay-out problems. This device can be used with a single external capacitor

The basic output pulse width is determined by selection of an internal resistor R_{INT} or an external resistor (R_X) and capacitor (C_X). Once triggered the output pulse width is independent of further transitions of the inputs and is a function of the timing components. Pulse width can vary from a few Nano-seconds to 28 seconds by choosing appropriate R_X and C_X combinations.

Inputs			Outputs	
A1	A2	B	Q	$\bar{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎎
↓	H	H	⎍	⎎
↓	↓	H	⎍	⎎
L	X	↑	⎍	⎎
X	L	↑	⎍	⎎

H = High Logic Level
L = Low Logic Level
X = Can Be Either Low or High
↑ = Positive Going Transition
↓ = Negative Going Transition
⎍ = A Positive Pulse
⎎ = A Negative Pulse

Fig. 6.three trigger inputs

The pulse width is essentially determined by external timing components R_X and C_X. For C_X >1000 pF the output is defined as:

$$T_W = K R_X C_X \quad (1)$$

where
[R_X is in Kilo-ohm]
[C_X is in pico Farad]
[T_W is in nano second]
[K = 0.7]

Power cycle OBC / S-band receiver with one second pulse, RX is chose 300k ohm, CX is chose 4.7uF.

3.4 Current sensing circuit

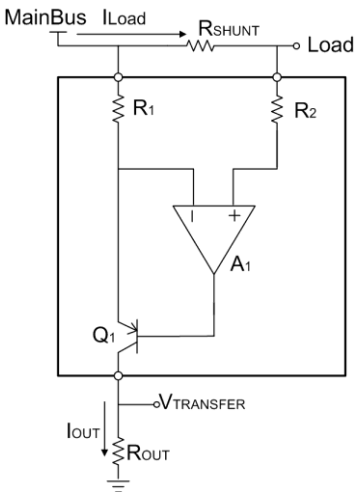

Fig. 7. High voltage current shunt monitor IC connection

Current sensing circuit is designed to catch load current value that provides for over current and current value evaluating. A high voltage current shunt monitor IC is chosen to achieve this purpose.

The current shunt monitor IC measures a small differential input voltage generated by a load current flowing through an external shunt resistor. The operational amplifier (A_1) is connected across the shunt resistor (R_{SHUNT}) with its inverting input connected to the MainBus side, and the non-inverting input connected to the load side of the satellite unit. Amplifier A_1 responds load current by causing Transistor Q_1 to conduct the necessary current through Resistor R_1 to equalize the potential at both the inverting and non-inverting inputs of Amplifier A_1. The current through the emitter of Transistor Q_1 (I_{OUT}) is proportional to the input voltage (V_{SENSE}), and, therefore, the load current (I_{LOAD}) through the shunt resistor (R_{SHUNT}). The output current (I_{OUT}) is converted to a voltage ($V_{TRANSFER}$) by using an external output resistor, the value of which is dependent on the input to output gain equation desired in sub-system requirements.

The transfer function of the current shunt monitor IC is

$$I_{OUT} = (gm \times V_{SENSE}) \quad (2)$$

$$V_{SENSE} = I_{LOAD} \times R_{SHUNT} \quad (3)$$

$$V_{TRANSFER} = I_{OUT} \times R_{OUT} \quad (4)$$

$$V_{TRANSFER} = (V_{SENSE} \times R_{OUT})/1000 \quad (5)$$

Where: gm = 1000 μA/V

3.5 Transistor feedback circuit

As overload or short-circuit takes place, the LCL[4] limits load current in a greatest acceptable value with trip-off time. LCL function is implemented with a simple Transistor feedback circuit. The BJT transistor is used to

control the gate length of power MOSFET according to the $V_{TRANSFER}$ magnitude. As the load current increases rapidly, $V_{TRANSFER}$ is proportional immediately. Therefore, BJT transistor starts to decrease the gate voltage (length) of power MOSFET that reduces the load current, also means $V_{TRANSFER}$ decreases. Finally BJT transistor maintains a control balance to power MOSFET; the feedback circle forms a limitation to the load current in a latching value. In order to get different LCL types, resistor R_1 and R_2 value can be adjusted by requirement.

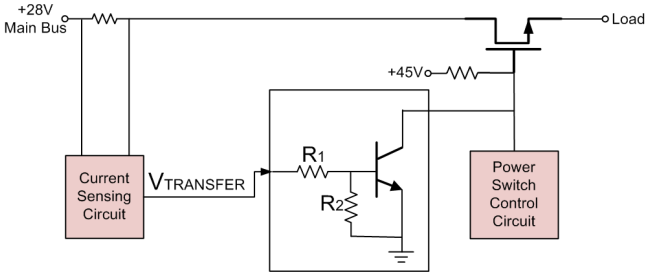

Fig. 8.BJT feedback circuit

3.6 Current monitor

Current monitor circuit can provide user to read load current value. The realizable method is using an OP amplifier that amplify $V_{TRANSFER}$ for corresponding current value. Each load has a max allowed current, current monitor output should within A/D converter max scale to avoid not appear desired current value.

In order to save PCB area, the same level outlets can share the current monitor by using an analog multiplexer. FPGA switches multiplexer to output every channel's current value to A/D converter.

3.7 Over current detector

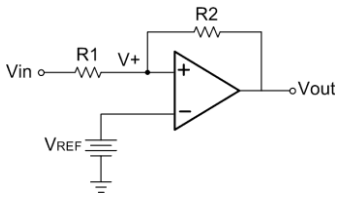

Fig. 9. Over current deector with Schmitt trigger

In Current Sensing Circuit, load current is transformed to $V_{TRANSFER}$ that can be compared in the Over Current detector. As $V_{TRANSFER}$ is higher than V_{REF} which means the load current is higher than the limit, Trip-off Load, the comparator [5] will output an over-current flag immediately to FPGA. The Schmitt trigger circuit also provides the Hysteresis [6] function to avoid error trigger by noise interference.

4 Measurement

A circuit evaluated board is designed to verify PD outlet function. This evaluated board includes power switch control circuit, current sensing circuit, transistor feedback circuit, over current detector and current monitor.

For functional testing, an electronic load is used to simulate a real satellite equipment load. Electronic load, Agilent N3300A (mainframe) and N3305A (500W E-Load module), can be set to sink arbitrary current from PD as desired.

According to each equipment power demands in satellite, PD outlet could be designed for different specifications, as showed in Table I. Chose Class C LCL be an example of testing. If overload or short-circuit happens, the LCL protection function will be trigged. For class C, the trip off time is 5ms ± 5% and LCL is set to 2.73 A± 20%.

Sent 3.3V TTL command to switch control circuit, power MOSFET can be switched and main bus voltage measured at outlet output. By using the electronic load to sink 3.0A from outlet, current sensing circuit transferred current to voltage, $V_{TRANSFER}$ that received by BJT feedback circuit. The LCL protected load current to keep current at 2.73A instantly as showed in Figure 8. At the same time, over current detector produced a flag which will be count by housekeeping interface (HKIF)'s FPGA in PCU EBB for Trip-off time countdown. After 5ms ± 5%, the FPGA can turns off the switch to terminate load current output.

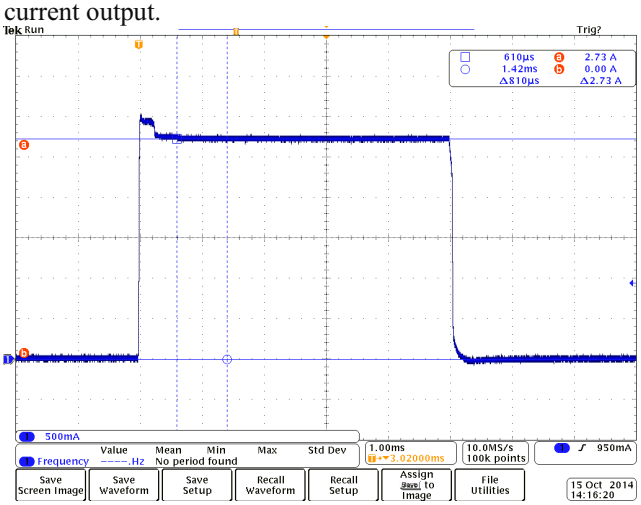

Fig. 10. Latching Current Limit measurement result

For current monitor test, using the electronic load to sink output and record the respond value of current monitor. These results of current monitor are linear, as table II shows. For PCU EBB, transmitting these analog data to a 12 bit A/D converter which can output digital hex data to HKIF's FPGA. According to Engineering Translation factor which wrote in Fly software, the current value can appear on display page.

Table 2. List of Outlet Types

Current	Measurement	Engineering Translation	Error
0A	0.05V	0.02A	NA
0.5A	1.103V	0.51A	2.0%
1.0A	2.176V	1.01A	1.0%
1.5A	3.257V	1.51A	0.60%
2.0A	4.340V	2.01A	0.50%
2.5A	5.467V	2.54A	1.60%
3.0A	6.600V	3.07A	2.30%

5 Conclusions

We present the PCU architecture description for Micro-Satellite and the PD circuit design in the PCU Elegant Breadboard (EBB) in this study. In order to verify the circuit design, an evaluated board was manufactured to provide measurement and fine-tuning for PD_EBB. According to evaluated board testing result, PD_EBB design has finished the circuit design, PCB fabrication is ongoing and functional checkout will execute sequentially.

PCU_EBB will be the first step for MicroSat mission, the follow-on PCU development will be engineer model (EM), Engineering Qualification Model (EQM) which will execute the Electromagnetic Interference (EMI) analysis, Thermal-Vacuum Testing, and vebration testing.

Through above Environmental testing, the PCU will continue to step in Fight Model (FM) which is real using in the MicroSat mission.

References

1 Networks [Online]. Available: https://en.wikipedia.org/wiki/Small_satellite#Microsatellites

2 Che-Cheng Huang, Jia-Jing Yeh, Zhe-Yang Huang, Chien-Kai Tseng "FORMOSAT-5 Satellite Power Protection Design," *Applied Mechanics and Materials,* Vol. 145, pp 536-541, Dec. 2011

3 Raymond A. Mack, Demystifying switching power supplies, Elsevier Inc. Austin, TX, USA,(2005), pp. 33

4 Earl Crandall, Power supply testing handbook: strategic approaches in test cost reduction, Kluwer Academic Pub, (1997), pp. 27

5 Herrick, Robert J., DC/AC circuits and electronics: principles & applications, Thomson Learning,(2002), pp. 378

6 U.A. Bakshi, A.P Godse, Analog Electronics, 1st ed., Technical Publications, (2009), pp. A7.