Extensive review on Supercapacitor cell voltage balancing

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Abstract. This paper explains about the supercapacitor cell voltage balancing circuits by comparing different topologies with regard to parameters like cost, balancing time, weight of the components used and control of switches. The advantage of supercapacitor over battery made to overcome weight and faster responding source problems. In supercapacitor bank cell voltages differ from each other which effects the performance of the device. Passive circuits consume power from cell for balancing but active circuits consume power from source. Many topologies are considered in this paper for different ratings and with different components. Balancing circuit is selected based upon total number of components in the balancing circuit, many components make circuit less reliable, complex and also increase the cost for balancing.

1 Introduction

Recent developments in graphene utilisation and manufacturing process made of the Supercapacitor (SC) demand rise [1]. SC a high power density source [2] when used in group like a bank for a high power requirement operation should be flawless. SC takes a span of seconds to pump the entire power to the load where time generally lies from 2 -15 seconds or so. Time of Power pumping demand is generally based on load requirement. Similar to alternators which pump power to power grid care is taken to make balance all alternators equally as required. Paralleling operation of alternator is dynamic in nature where voltage and frequency variations ±5% are observed. SC which deal with individual voltages of 2.6-2.85V [2] a small variation in voltage due to internal resistance or change in temperature of cell, change in a small part of composition of chemical and so on will lead to imbalance of power pumping. When used in a SC banks a small variations in any parameters mentioned above make them to unequal power pumping [4]. These parameters leads to discharge faster and SC cells to get overloaded due to imbalance and pump low power than their designed value. Adding a addition circuit which make all SC cells to balance and pump approximately equal power so that all cells are equally loaded and fulfill the load requirement for a given time. So, SC balancing circuit are designed to make effective and equally utilization of all cells in a SC bank and also improve life span of SC [5] by equally loading each cell.

2.Supercapacitor balancing using different topologies

SC balancing circuit are designed based on many parameters consideration taking in account like fast balancing, low source current to balance, easy to operate, effective voltage balance, bulk cells balancing, less components, and many more. But based on topologies selected the above parameters vary and decide the circuit functions and cost of module. Balancing circuit can roughly classified into two types namely
1) Passive circuits and

2) Active circuits

Passive circuits are those circuits which uses resistors and other elements to make balance of bank. But this method is a older and consume power from SC to balance. Active method includes many components on proper coordination between switches balancing takes place properly and effectively. But energy to balance cell voltage is taken from source.

2.2 Passive Balancing Circuits

2.2.1 Topology 1

Topology 1 uses a resistors connected in a series with a switch connected in parallel with SC [6]. These circuit when used for a bigger banks becomes complex as each SC cell voltage differ from each other. So each switch need to operated independently Fig. 1. shows the circuit diagram used for topology 1 where resistor (R), Super Capacitor (C) and switch (S). These kind of topology discharges in resistors to balance by which SC is not effectively used and time to balance the SC is also more.

2.2.2 Topology 2

Topology 2 uses a Zener diode in parallel with SC. But use of Zener diode make use of power from SC to balance cells. Apart from that a strong temperature dependency of

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Zener diode creates a drawback to the topology [7]. Time to balance the SC is also huge as no external source is used to balance it. Fig. 2. shows the balancing of SC using Zener diode.

2.2.3 Topology 3

Topology 3 is a advanced version of topology 1 where a proper coordination between cells are done by communicating between cell to cell. A controller senses cell voltage and controls according to the requirement [8]. A cyber layer is used in between to balance all cells. A closed loop operation is used in the topology making it complex and also costly. Fig.3. show the circuit diagram used for the topology 3. Cyber layer used to control the operaton make it to costly and also complex. Communication between cells plays a major role. Any mis-match of communication can damage the cell.

2.3 Active balancing circuits

2.3.1Topology 4

Topology 4 uses a DC/DC converter. Converters operates in buck/boost mode based on the cell voltage in the bank based on the average voltage of bank. But when used for bulk circuits it becomes more complex as individual circuits are required and each cell requires converter and it makes circuit complex, more weight and costly [9]. Fig.4. shows the balancing of topology 4. As the cells are balanced between each other it takes more time to balance. Topology used for many cells makes it costly and complex but high efficient.

2.3.2 Topology 5

Topology 5 is used for high power applications. Fig.5. shows the topology 5 balancing circuit. Toplogy 5 is high efficient reaching peak effficency of 91-95%. The charging current (I_{ch}) is used to charge the cells intially and balacing current (I_{bal}) is used to balance alternatively [10]. Time to balance all the cells is around the 160 secounds. But in fast charging mode where on pumping more current, makes time to balance lower. Balancing circuit designed uses a multi winding transformer in circuit. Windings required for the circuit is given by n+1. where n = number of SC cells in balancing circuit.

2.3.3 Topology 6

Topology 6 is a high efficient than any other topologies mentioned in this paper. Its peak efficiency lies near by 98.4%. Topology uses circuit in buck/boost modes to balance faster. Fig.6. shows the topology 6 balancing circuit [11]. Inductor is used as a part of converter. Circuit balances the voltage faster but it is costly when viewed from high end SC banks**.**

2.3.4 Topology 7

Topology is operated by a controller but with special source funtionality and with OCET switches. This make it different from other topologys but time to balance the cells voltage lies between 80 seconds. Fig.7. describes the balancing circuit of Topology 7. Controller operates according to cell voltage and other parameters [12]. But the balancing of cell is applied only between two cells. Fig. 7 shows circuit diagram for topology 7.

2.3.5 Topology 8

Topology 8 balancing is done on a hybrid power source. As the cells voltage of batteries also differs they need yet to be balanced [13]. These sources are placed in parallel to operate independently. Topology uses a same switch arrangement to balance batteries and also SC cells. Time to balance all those capacitors lies between 120 seconds which is more for when viewed from a automobile sector. As dynamic power pumping is needed to drive the electric vechile based on road profile for a urban traffic balancing need to be faster. Operating 120 secounds to balance cell voltage makes the vechile to decrease SC bank life span as balancing of cell voltage is not completed for a urban type road profile. Fig. 8 shows the circuit for topology 8.

2.3.6 Topology 9

Topology 9 is used for bulk operation, where the circuit designed is for 512 cells balancing. As many cells are used control becomes complex and balancing time is more. Fig. 9. shows circuit for Topology 9. Buck converter is used to provide a constant voltage of 24V. Active clamped circuit are used to make the balancing operation. Each cell voltage is balanced separately by a logic, by calculating a average voltage [14]. Later cells with higher voltages try to balance with lower voltages by sharing the voltage and reach the average voltage. For a bank of 512 cells 25A of balancing current is too small making it to balance slowly. Voltage variation of 1.2% was observed after balancing the cells.

2.3.7 Topology 10

Topology 10 is similar to the a passive controlled resistor circuit as mentioned in Topology 1. In these topology a capacitor is used instead of a resistor [15]. The advantage of the topology is that it tries to balance the circuit faster compared to topology 1. Fig. 10 shows circuit for Topology 10. Topology arrangement is complex where seen from controlling part. A small capacitor is placed parallel to the SC as "Equilibrium capacitor"(C'). Equilibrium capacitor make the SC to balance by transfer of power between them. Equilibrium capacitor make the control operation a complex to control.

2.3.8 Topology 11

Topology is a simple circuit and operates with lower currents. The circuit uses RLC tank elements to balance operating below resonant frequency [16]. All SC form a grid where balancing of all cells take place equally. Balancing of all cells with variation of 50-100mV. Fig. 11 shows the circuit diagram of topology 11. RLC tank circuit decides parameters like balancing time, balancing voltage, balancing current and switch frequency. So care

need to be taken while designing the RLC tank. As the voltage balancing is accurate it takes 350 seconds. The circuit developed can be applied to 1000 times higher rated than cells used in the circuit.

2.3.9 Topology 12

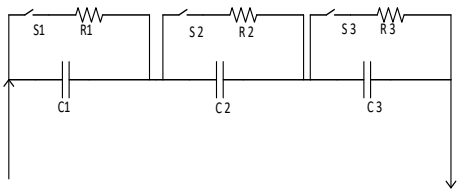
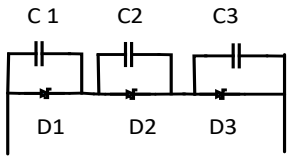
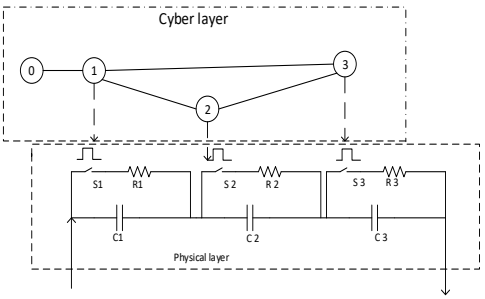
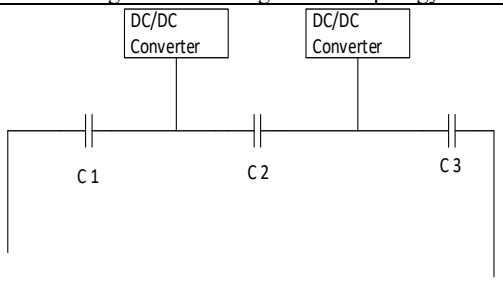
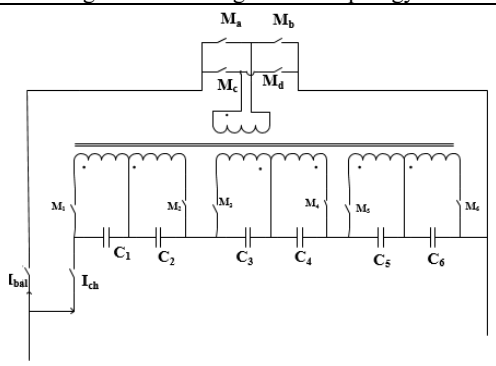
Topology 12 is a simple arrangement of cells in series and connected with the source and switches. Logics applied between the switches make circuit to balance in a different manner [17]. Some variation in control generates a high ripple which damages cells. A common logic between switches could be developed whatever the unbalancing of cell voltage might be. Perfect logic make the cells to balance safely and faster. Main advantage of the topology is that it can handle from low to high power cells. This topology uses many switches interconnection which makes the balancing operation faster and time to balance depends on the logic used and also on frequency of operation. Fig. 12 shows the circuit diagram used for topology 12.

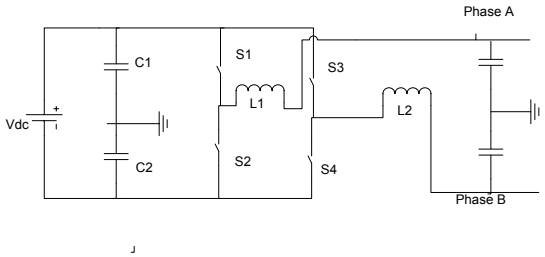
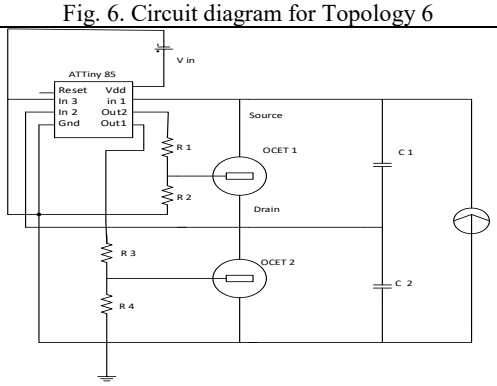
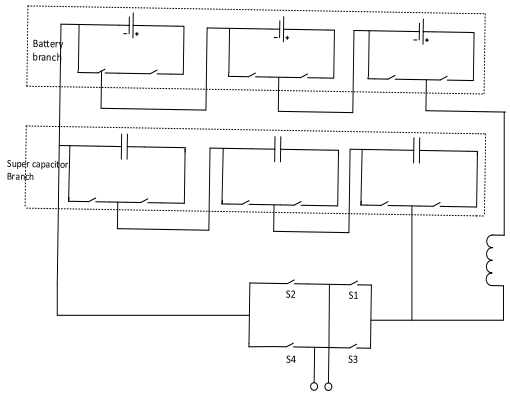
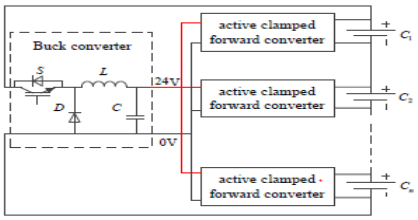
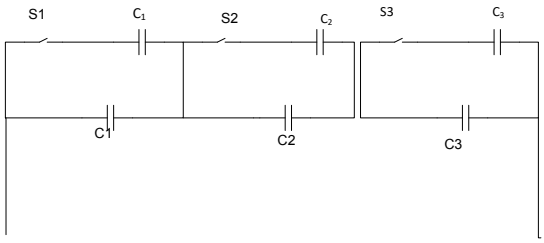
All the 12 topologies are compared in Table. I & II on various parameters. Based on circuit arrangement and components used in topologies making the balancing operation different from each other which can be observed in Tables listed below. Based on the current flowing in the circuit between the elements decides the balancing. A higher voltage to the circuit make the SC cells to damage as SC are voltage sensitive elements. Lower the voltage makes the balancing slow. So a proper voltage need to be applied to make the balancing faster and operate in a safer region.

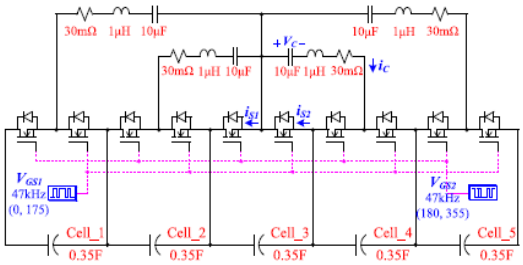
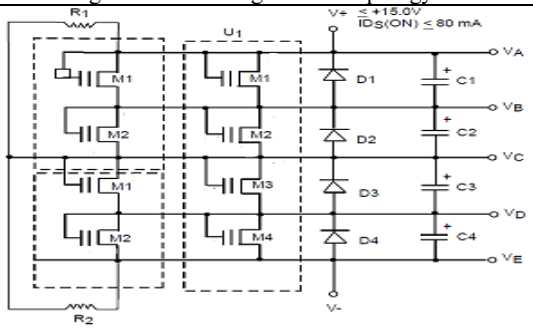
Table I. comparison of different topologies in various parameters

Topology	**Switches used**	**Balancing time**	**External components**	**Control of balancing circuit**	**Weight of circuit**	**Cost of circuit**
Topology 1	one / cell	High	one Power resistor/ cell	easy	light	Low
Topology 2	zero	High	Nil	No switch	light	Low
Topology 3	one / cell	Medium	Resistor	siimple	light	Moderate
Topology 4	one converter/ cell	Less than medium	dc/ dc converter /cell	easy	heavy	High
Topology 5	one/cell + four/ module	Medium	Multi winding transformer.	easy	heavy	High
Topology 6	two switches/ cell	Medium	one capacitor/ cell	easy	light	High
Topology 7	one switch/ cell	Low	2Resistor, 1 capacitors/ cell	complex	light	High
Topology 8	two switch/cell	Low	Nothing	complex	light	Moderate
Topology 9	Four switches/cell	Low	Forward converter/cell	complex	heavy	High
Topology 10	one switch/cell	Medium	Equilibrium capacitor/cell	complex	light	Moderate
Topology 11	Two swiitch/cell	Medium	RLC tank circuits	simple	light	Moderate

Table 2. Comparison of different topologies on Switch based parameters and circuit.

Topology	Application	Types of circuit	Type of Switch	Circuit arrangement
Topology 1	Low	Passive	Mosfet	 Fig. 1. Circuit diagram for Topology 1
Topology 2	Low	Passive	No switches	 Fig. 2. Circuit diagram for Topology 2
Topology 3	Low	Passive	Mosfet	 Fig. 3. Circuit diagram for Topology 3
Topology 4	Medium	Active	Mosfet	 Fig. 4. Circuit diagram for Topology 4
Topology 5	Medium	Active	Mosfet	 Fig. 5. Circuit diagram for Topology 5

Topology 6	Medium	Active	IGBT	 Fig. 6. Circuit diagram for Topology 6
Topology 7	Medium	Active	OECT	 Fig. 7. Circuit diagram for Topology 7
Topology 8	High	Active	Mosfet	 Fig. 8. Circuit diagram for Topology 8
Topology 9	High	Active	Mosfet, IGBT	 Fig. 9. Circuit diagram for Topology 9
Topology 10	High	Active	Mosfet	 Fig. 10. Circuit diagram for Topology 10

Topology 11	Low	Active	Mosfet	 Fig. 11. Circuit diagram for Topology 11
Topology 12	Low - High	Active	Mosfet (or) IGBT	 Fig. 12. Circuit diagram for Topology 12

3. Conclusion

This paper compares different topologies of Supercapacitor voltage balancing circuit considering balancing time, circuit complexity, elements used, weight of circuit, control strategy, cost and types of switches used. Based upon the arrangement and the logic used to balancing the circuit voltage balancing between cells behavior changes. Faster balancing, high efficient balancing, less complex and high power bank circuits are mention in the topologies. Major focus of the paper is on faster balancing of cells, less complex, lighter weight and cheap each topologies fulfill some parameters. But Topology 12 fulfill faster volatage balancing, lighter weight, cheaper and less complex parameters and can be used for low to high power applications.

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