Novel Frequency-Doubling Modulation and Control Strategy for Three-Level Full Bridge based Power Electronic Traction Transformers

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Abstract. Power electronic traction transformers (PETTs) are widely investigated to substitute bulky line frequency transformers in railway traction system presently. This paper adopts the three-level topology for both grid-side cascaded converters and primary-sides of LLC resonant converters. The cascade number is reduced by half as well as isolated transformers compared to the traditional two-level configuration. Less cascade number of modular converters leaves relatively more space for electric insulation implementation, which is beneficial to PETTs in terms of the limited installation space in the train. A frequency-doubling modulation strategy for LLC resonant converters is proposed, which can enable the operating frequency of isolated transformers two times higher than the switching frequency to further reduce the transformer size without increasing the switching loss. Meanwhile the proposed modulation strategy can realize the capacitor voltage balance autonomously as well. Additionally, the control strategy of cascaded rectifiers and key parameter design guideline of LLC resonant converters are also introduced.

1 Introduction

Recently, medium frequency power electronic traction transformers (PETTs) have attracted increasing attention of High-speed train (HST) industry due to its compact magnetic component, light weight, power quality control and other additional functionalities [1].

The world's first ever 1.2MW PETT developed by ABB has been successfully installed and commissioned on a locomotive for 15kV, 16.67Hz railway grid [2-4]. Nevertheless, the proliferation of PETT encounters severe challenges when referring to the 25kV, 50Hz railway grid, because of higher voltage rating, line frequency and insulation requirement. Following the Standard IEC 60146-1-1-2009, in a single phase 25kV railway grid, the uppermost modular converter (Module I highlighted in Fig.1) must perform uninterruptedly in the 85kV/50Hz condition for one minute, where the testing voltage is applied between the insulation shell of Module I and the ground. To fulfil the standard, larger creepage distance or thicker insulation shells are required, which is space consuming and unacceptable. Reducing the number of cascaded converters will relatively enlarge insulation distance in the same installation space and consequently relieve insulation pressure to some extent.

Theoretically, less cascade number and/or higher isolated transformer operating frequency can both lead to a smaller size for PETT.

Silicon carbide (SiC) devices can maintain high switching speed even at high voltages, but presently are not suitable for PETT in terms of EMI and cost issues. Due to limited voltage blocking capabilities of contemporarily available semiconductor devices, 6.5 kV IGBTs are often the choice in order to keep the modular number at minimum [5, 6]. LLC resonant converters are commonly employed to mitigate switching loss and increase the switching frequency. Nonetheless, the switching frequency is still limited considering high voltage stress, switching loss and shoot-through risk. In [4] the switching frequency of 6.5kV IGBTs operates at 1.8 kHz under a 225 kW condition, which is not yet high enough to further reduce the transformer volume to a desired range. [7] proposes a modulation for three-level LLC resonant converters to make the transformer operating frequency two times of the switching frequency. Nevertheless, the output voltage is only one-fourth of the dc-link voltage. A small magnetizing inductance is required to realize ZVS of primary side switches, but it will increase the transformer loss.

This paper adopts the diode-clamped three-level topology for both grid-side cascaded converters and primary-side of LLC resonant converters [8~12]. Resultantly, the total cascade number as well as the isolated transformers is reduced to half compared to the traditional two-level structure. Moreover, a novel frequency-doubling modulation strategy for LLC resonant converters is proposed, which can not only push the operating frequency of the isolated transformers twice as high as the switching frequency but also regulate the capacitor voltage balance autonomously. In addition, the

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control strategy in d-q synchronous rotating reference frame of cascaded rectifiers and key parameter design guideline of LLC resonant converters are also introduced. Simulations are shown to verify the theoretical considerations and findings.

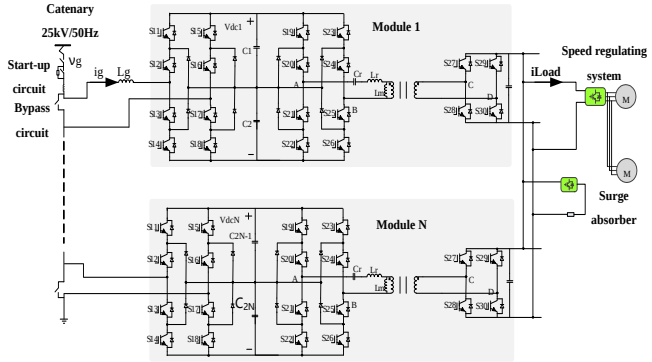

Fig. 1. The structure of the adopted PETT.

2 Topology of PETT

PETT is implemented by means of cascaded modular converters in connection directly to the railway grid through a smoothing choke inductor. As illustrated in the shadow block of Fig.1, the submodule put forward in this paper consists of a single phase diode-clamped three-level rectifier and an LLC resonant converter. The primary side of the LLC resonant converter also employs diode-clamped three-level full bridge structure sharing capacitors with the front-end rectifier. In contrast, the secondary side converter still prefers the two-level full bridge topology. The input series capacitors C_1 and C_2 with the same capacitance clamp the primary switch voltage stress to half of the input voltage. L_r, C_r and L_m are resonant inductor, resonant capacitor, and transformer magnetizing inductor respectively, which constitute the resonant tank. N is the cascade number of submodules.

The dc-link voltage of the front-end rectifier is 7.2kV, where 6.5kV IGBT devices are used. While the output dc-link voltage is 1.8kV, in which 3.3 kV IGBTs with lower voltage rating but higher switching frequency are taken. Accordingly, the cascade number and the isolated transformers are decreased to half of the common two-level configuration based PETT. Herein it should be noticed that the voltage stress of semiconductors are the same as the ones in two-level converters.

3 Modulation and control strategy

3.1 Proposed frequency-doubling modulation for three-level LLC resonant converter

Despite that LLC resonant converter features soft commutation and less switching loss, the switching frequency cannot be pushed higher arbitrarily in high power applications. A novel frequency-doubling modulation strategy for the three-level LLC resonant converters is put forward to solve the above dilemma.

For simplicity, take a single module in Fig. 2(a) for instance to demonstrate the modulation strategy. As shown in Fig.2 (b), D_S_{19} to D_S_{22} are the drive signals of switches S_{19} to S_{22}. D_S_{19} has a duty cycle of 0.25. While D_S_{20} has a duty cycle of 0.75 and its rising edge is delayed by a half cycle of D_S_{19}'s. D_S_{21} is a complementary signal of D_S_{19}, and D_S_{22} is a complementary signal of D_S_{20}. Similarly, D_S_{23} to D_S_{26} are the drive signals of switches S_{23} to S_{26}. D_S_{23} has a duty cycle of 0.25, while D_S_{24} has a duty cycle of 0.75. Both the rising edges of D_S_{23} and D_S_{24} are lagged by three quarters of a switching period of D_S_{19}'s. D_S_{25} is complementary to D_S_{23}, and D_S_{26} is complementary to D_S_{24}.

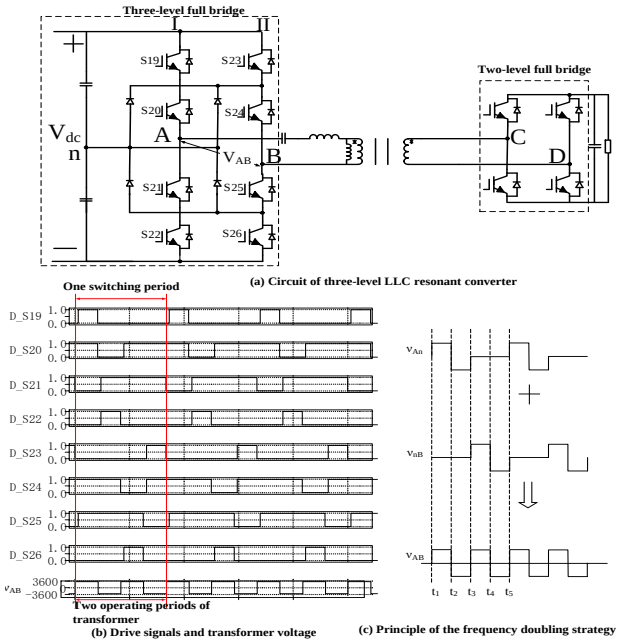

Fig. 2. The proposed modulation strategy for three-level LLC resonant converters

Fig. 2(c) shows the principle of the frequency doubling strategy. When the switching devices of the three-level half bridge I are driven by gate signals D_S_{19}~D_S_{22}, the voltage potential v_{An} between the neutral points of Bridge I and the two capacitors is correspondingly a square wave in the first half switching period. Then v_{An} keeps zero level in the last half switching period. The magnitude and frequency of v_{An} are equal to $V_{dc}/2$ and switching frequency respectively. Likewise, when the switching devices of the three-level half bridge II are driven by gate signals D_S_{23}~D_S_{26}, the voltage potential v_{nB} between the neutral points of the two capacitors and Bridge II is zero level in the first half switching period. Subsequently v_{nB} becomes a square wave in the last half switching period. According to the superposition principle, the output voltage of the three-level full bridge v_{AB} is a square wave, of which magnitude is $V_{dc}/2$. Besides, its frequency is twice the amount of the switching frequency. It can be clearly seen that the modulation strategy indeed achieve frequency doubling of the transformer without increasing the switching frequency.

The magnetizing current of LLC resonant converter is mainly dependent on the output voltage and remains nearly constant. From Fig. 2(b), (c) and Fig. 3, due to the

symmetry of both the circuit topology and the proposed modulation, the two series capacitors have the same charging and/or discharging time intervals, which results in more energy transferred to the load from the capacitor with higher voltage. Therefore, the voltage balance can be achieved autonomously.

The conducting time of inner switches of the three-level bridge is longer than outer switches' of the same three-level bridge. Consequently the conducting loss of inner switches is larger, which should be carefully considered when designing cooling systems. In order to prevent the switches from being damaged by the full dc bus voltage when the LLC resonant converter shuts down, the outer switches of three-level bridges must be turned off ahead of the inner ones. The proposed modulation strategy is applicable in both traction mode and braking mode. It allows the power flowing from primary side to the secondary side of the transformer and vice versa.

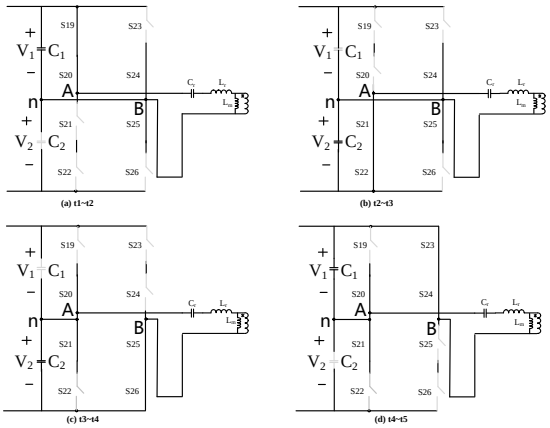

Fig. 3. Equivalent circuits of LLC resonant converter in different operating modes under the proposed modulation strategy

3.2 Control of grid-tied cascaded single phase three-level rectifiers

A dual closed-loop control strategy including dc bus voltage outer loop and grid-tied current inner loop is employed for a good power flow and dc voltage tracing effect. All the two control loops are implemented in the single phase virtual d-q synchronous rotating reference frame. Consequently, the grid-tied current steady-state error can be effectively minimized by PI regulator. The control block diagram is shown in Fig. 4.

The control strategy of cascaded rectifiers is mainly composed of four parts, which are (1) Fig. 4(a) d-q synchronous rotating reference transformation of grid voltage and current, (2) Fig. 4(b) the overall dc-link voltage control of cascaded rectifiers, (3) Fig. 4(c) the grid-tied current control and (4) Fig. 4(d) the generation of gate driving signals.

Second-order generalized integrator (SOGI) is used to generate the corresponding virtual variables of grid voltage vg and grid-tied current ig in the Beta axis. The overall dc-link voltage control is on the basis of instant power balance between the input side and output side of the rectifiers. The overall dc-link voltage square is taken as the objective variable which is linearly proportional to the system active power. A low-pass filter is used to eliminate the side effect of the double line frequency ripple of the dc-link voltage on the grid-tied current. To achieve the balance of each rectifier's dc-link voltage, the average demand voltage is modified separately as in Fig. 4(d). Carrier phase shift (CPS) based single phase Space vector pulse modulation (SVPM) is carried out to increase the equivalent switching frequency. Define the carrier of the Xth cascaded rectifier as Carrier X, and thereby the angular difference between Carrier X and Carrier 1 is $\frac{(X-1)2\pi}{N}$.

4 Design of key parameters

4.1 Resonant tank design

Based on fundamental harmonic approximation (FHA), the gain of an LLC resonant circuit is obtained as

$$G = \frac{1}{\sqrt{[1+\frac{1}{k}(1-\frac{1}{f^2})]^2+(f-\frac{1}{f})^2Q^2}} \quad (1),$$

where $k=\frac{L_m}{L_r}$, $f=\frac{f_s}{f_r}$, $f_r=\frac{1}{2\sqrt{L_rC_r}}$, $Q=\frac{\sqrt{L_r/C_r}}{R_{eq}}$, $R_{eq}=\frac{8n^2}{\pi^2}R_{load}=\frac{8n^2}{\pi^2}\frac{V_o^2}{P_{load}}$,$V_o$ is the output dc voltage, n is the turn ratio, P_{load} is the load power, f_r is the resonant frequency of L_r and C_r. It should be noted that f_s is the transformer operating frequency which is two times higher than the switching frequencyf_{sw}. The voltage gain curves of LLC converter with variable k and Q are given in Fig. 5.

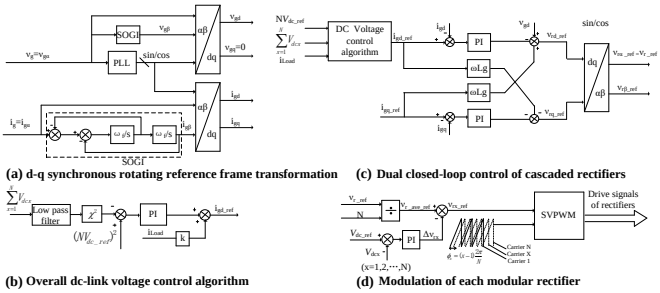

Fig. 4. Control block diagram of grid-tied cascaded rectifiers.

For single-phase traction power systems, there is inherently double-line-frequency (2ω) ripple in the dc-link voltage. The 2ω ripple will lead to ZVS failure and introduce hazardous beat components into the motor current. Voltage regulation by varying the operating frequency can eliminate the adverse effect of the 2ω ripple to some extent.

The transient switch turn-off processes are given in Fig. 6 and Fig. 7, where C_{oss} is the output capacitor of the switch and toff is the switch turn-off time duration. For simplicity, assume all the switch output capacitors have the same value, the turn-off current remains constant, and the IGBT current decreases linearly.

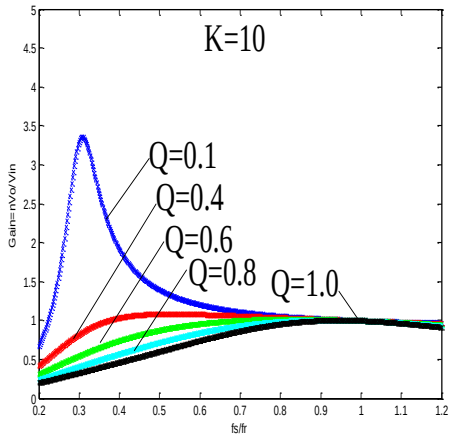

Fig. 5. Voltage gain curves of LLC converter

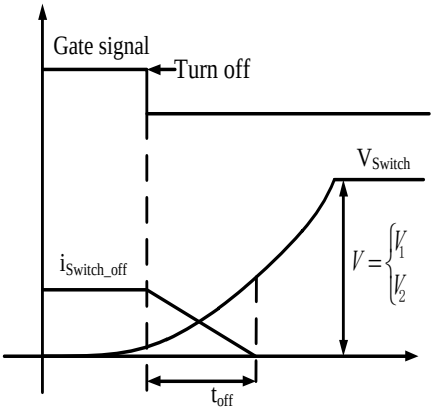

Fig. 6. Voltage and current curves during the switch turn-off process

The commutation currents of the turn-off switch devices and switch output capacitors are shown as

$$i_{switch_{off}}(t) = I_{off}\left(1-\frac{t}{t_{off}}\right) = \frac{nV_o}{4L_m f_r}\left(1-\frac{t}{t_{off}}\right) \quad (2),$$

$$i_{coss1}(t) = -i_{coss2}(t) = \frac{t}{2t_{off}} I_{off} \quad (3),$$

$$i_{coss}(t) = \frac{t}{t_{off}} I_{off} \quad (4),$$

where I_{off} is the switch device current at the turn-off moment and t_{dead} is the dead time.

Thereby the voltages of the two series turn-off switches in Fig. 7(a) and (c) are

$$V_{switch\_1}(t) = \frac{nV_o t^2}{16C_{oss}L_m f_r t_{off}} \quad (5).$$

While the voltages of the single turn-off switch in Fig. 9(b) and (d) are

$$V_{switch\_2}(t) = \frac{nV_o t^2}{8C_{oss}L_m f_r t_{off}} \quad (6).$$

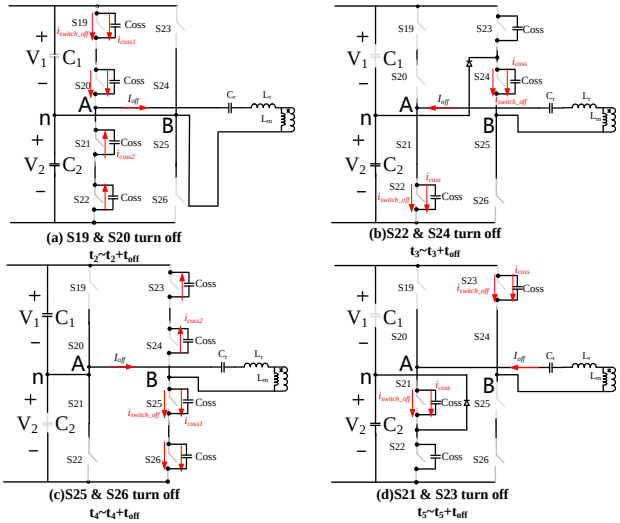

Fig. 7. Equivalent circuits during the switch turn-off process

Combining (2)~(6), the switch turn-off loss of all three-level LLC converters of PETT in one switching period T_{sw} can be calculated as

$$P_{turn-off_{loss}}(t) = N\frac{[2(\int_{t_2}^{t_2+t_{off}} dt + \int_{t_4}^{t_4+t_{off}} dt)V_{switch_1}(t)\, i_{switch_{off}}(t) + 2(\int_{t_3}^{t_3+t_{off}} dt + \int_{t_5}^{t_5+t_{off}} dt)V_{switch_2}(t)\, i_{switch_{off}}(t)]}{T_{sw}}$$

$$= N\frac{(nV_o)^2 t_{off}^2 f_{sw}}{64C_{oss}L_m^2 f_r^2} \quad (7)$$

where N is the cascade number of modules in PETT.

As a contrast, the switch turn-off loss of all two-level full bridge LLC resonant converters of PETT can be calculated as

$$P_{turn-off_{loss}}(t) = 2N\frac{(nV_o)^2 t_{off}^2 f_s}{192C_{oss}L_m^2 f_r^2} = N\frac{(nV_o)^2 t_{off}^2 f_{sw}}{48L_m^2 f_r^2} \quad (8),$$

where f_s is the switching frequency of the two-level full bridge LLC converter.

It can be noted that the overall switch turn-off loss of LLC resonant converters in this paper is reduced compared to the traditional LLC resonant converters. From (7), the primary side switch turn-off loss is inverse proportional to L_m^2. Increasing L_m will reduce the turn-off loss as well as the switch turn-off current but may result in the failure of ZVS. Thus the design of L_m must comprehensively consider both the turn-off loss and the ZVS realization.

4.2 Dead-time optimization

To guarantee ZVS turn-on of primary side switches, two requirements must be satisfied which are (1) having enough high turn-off current to completely charge or discharge the stray capacitors of switches and (2) having no inverse resonant current during the dead time. The corresponding inequalities are given as

$$8L_m f_r C_{oss} \le t_{dead} \quad (9),$$

and

$$0 \le \frac{nV_o}{4L_m f_r}\cos(\omega_r t_{dead}) - [(V_{in} - nV_o)\sqrt{\frac{L_r}{C_r}} + \frac{\pi I_{load} f_r}{2nf_s} + \frac{n\pi V_o}{8L_m}(\frac{1}{f_s} - \frac{1}{f_r})]\sin(\omega_r t_{dead}) \quad (10),$$

where $C_{oss}$is the switch device stray capacitance, $t_{dead}$is the dead time, $I_{load}$is the load current.

Consequently the dead time range can be determined according to (9) and (10).

5 Simulation verification

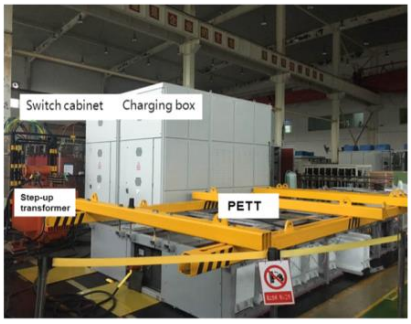

Fig. 8. The prototype of the proposed PETT

A prototype of the proposed PETT is shown as in Fig.8. The total weight of one 150 kW transformer with insulating cement is 80 kg, which is only equal to the weight of transformer in the traditional two-level topology. At present, we are just conducting the insulation test and some basic electrical tests. The control strategy has not been implemented in the prototype yet. Some simulation results are used to provide the validation of the proposed modulation method and control strategy.

Table1. Key parameters of simulation model

Cascade number N	3	Switching frequency of LLC converter	2.5kHz
Input inductor Lg	12 mH	Frequency of transformer fs	5kHz
Capacitors C1,C2	1.2 mF	Dead time	5 us
Output capacitor Cout	1.0 mF	Turn-off time delay between the inner and outer switches of three-level bridge	0.5 us
Magnetizing inductor Lm	5.0 mH	Turning ratio n	2:1
Resonant inductor Lr	200 uH	Primary dc-link voltage Vp	7.2 kV
Resonant capacitor, Cr	3.52 uF	Output dc-link voltage Vout	1.8 kV
Switching frequency of rectifiers	2 kHz	Overall output power Pout	450 kW

Table 1 gives the simulation parameters of the proposed PETT. There are three rectifiers in series connected to the grid and three LLC resonant converters paralleled on the dc output side. The control strategy and modulation methods are performed as the description in previous sections.

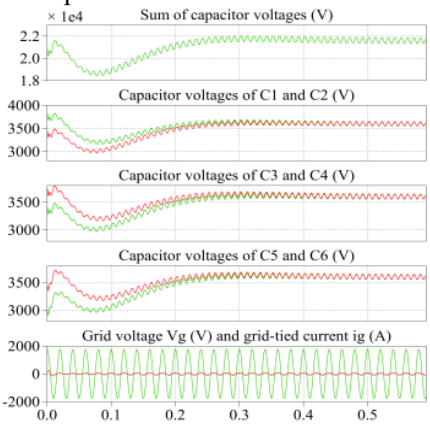

Fig. 9. Waveforms of grid & cascaded rectifiers

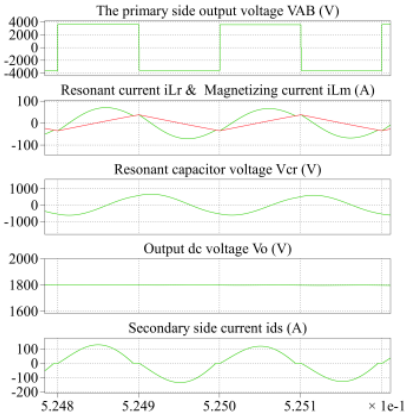

Fig. 10. Waveforms of LLC resonant converters

Fig.9 gives waveforms of grid and cascaded rectifiers in traction mode. In order to verify the capability of the control algorithm of balancing the states of charge of the capacitors, the simulation has run starting from an unbalanced condition. From the simulation results, the modulation strategy can balance the capacitor voltages autonomously without additional control and circuits. The grid voltage displayed here is attenuated to one-tenth of the real value. Fig.10 shows the waveforms of LLC resonant converter. The secondary side current waveform demonstrates that the diodes on the secondary side realize zero-current turn-off.

Fig.11(a)~(d) are voltage and current waveforms of Switch S_{19}~S_{26}. All the switch voltages are no higher than $V_{dc}/2$ when they are off. The voltages of Switch S_{19} and S_{20} drop to $V_{dc}/4$ when S_{22} is off. Likewise, the voltages of Switch S_{25} and S_{26} drop to $V_{dc}/4$ when S_{23} is off. In Fig. 11(a), the frequency of output voltage v_{AB}, which is also the operating frequency of the isolated transformer, is twice as high as the switching frequency. In Fig. 11 (b) and (d), the current at the switch turn-on moment is negative which means the anti-paralleled diode of the switch is conducting and the switch voltage is clamped at zero. Therefore the ZVS of switches on the primary side is achieved.

Fig.12 gives waveforms of grid and cascaded rectifiers in braking mode. In this situation, the train kinetic energy is feedback to the grid. The phase of grid-tied current is opposite to the grid voltage. The FFT analysis of grid-tied current verifies that the equivalent switching frequency of three cascaded rectifiers is pushed to 6 kHz by CPS. The grid voltage displayed here is attenuated to one-tenth of the real value. Fig. 13 is the waveforms of LLC converter in braking mode. The waveforms are similar to those in traction mode. By contrast, the intersections of the magnetizing current and resonant current are located in $[0,\pi/2]$ and $[\pi,3\pi/2]$ instead of in $[\pi/2, \pi]$ and $[3\pi/2,2\pi]$. Fig. 14(a)~(f) are voltage and current waveforms of Switch S_{19}~S_{26} in braking mode. All the switch voltages are no higher than $V_{dc}/2$ when they are off. The voltages of Switch S_{19} and S_{20} drop to $V_{dc}/4$ when S_{22} is off. Likewise, the voltages of Switch S_{25} and S_{26} drop to $V_{dc}/4$ when S_{23} is off. In Fig. 14(a), the frequency of output voltage v_{AB}, which is also the operating frequency of the isolated transformer, is twice as high as the switching frequency.

In braking mode, the primary side three-level converter is mainly operating as an uncontrolled diode rectifier. The current at the switch turn-on moment is negative which means the anti-paralleled diode of the switch is conducting and the switch voltage is clamped at zero as shown in Fig. 14(b) and (d).Therefore the ZVS of switches on the primary side is achieved. Fig. 14(e) and (f) are the voltage and current waveforms of switch S_{27} ~S_{30} on the secondary side. The current reaches zero before the switch turn-off, which means the ZCS of switches on the secondary side is achieved. High frequency ripple voltage in the switch voltage is generated by the resonance between stray capacitors of the secondary side switches and the primary side resonant tank. The high frequency ripple can be suppressed by increasing the capacitor of the primary side resonant tank. Selecting a larger resonant capacitor (or smaller$\sqrt{L_r/C_r}$) is consistent with the parameter design suggestion in Section IV.

6 Conclusions

Considering the limited installation space of PETT in HSTs, the diode-clamped three-level topology was applied for both grid-side cascaded converters and the primary-side of LLC resonant converters. The total cascade number and isolated transformers are reduced to half compared to the traditional two-level structure. This paper proposed a novel frequency-doubling modulation strategy for LLC resonant converters, which can not only push the operating frequency of the isolated transformers twice as high as the switching frequency but also regulate the capacitor voltage balance autonomously. Thus the isolated transformer can be reduced as well as the switch turn-off loss compared to the traditional two-level PETT. In addition, the control strategy in d-q synchronous rotating reference frame of cascaded rectifiers and key parameter design guideline of LLC resonant converters were also illustrated.

The influence of the double-line frequency ripple on LLC resonant converter, the loss of clamping diodes in three-level converters and the high frequency voltage ripple of the secondary side switches are to be further investigated in the next stage.

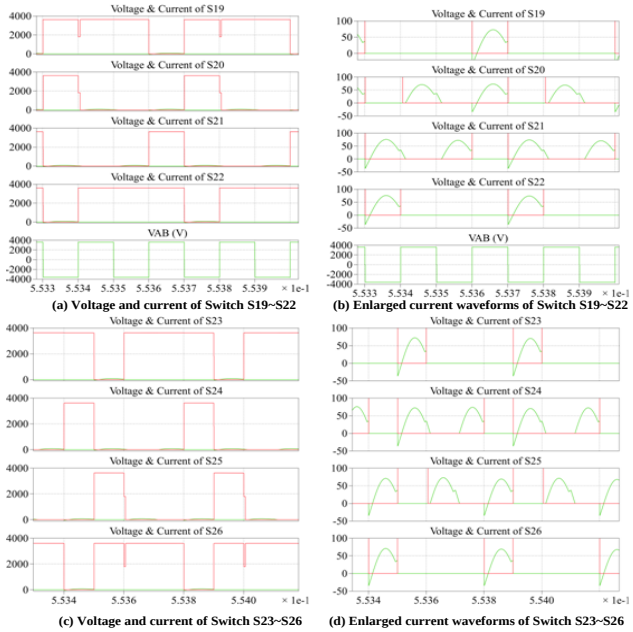

Fig. 11. Voltage and current waveforms of Switch S19~S26

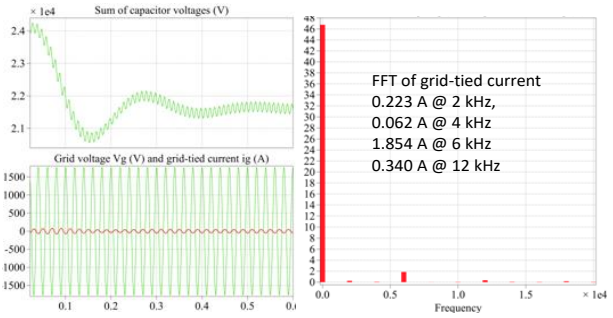

Fig. 12. Waveforms of grid and cascaded rectifiers in braking mode

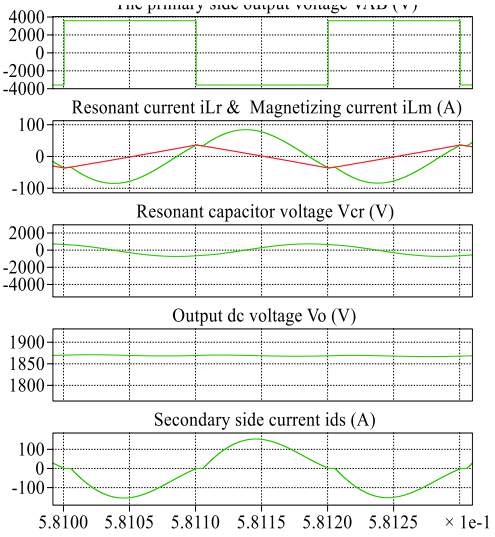

Fig. 13. Waveforms of LLC converters

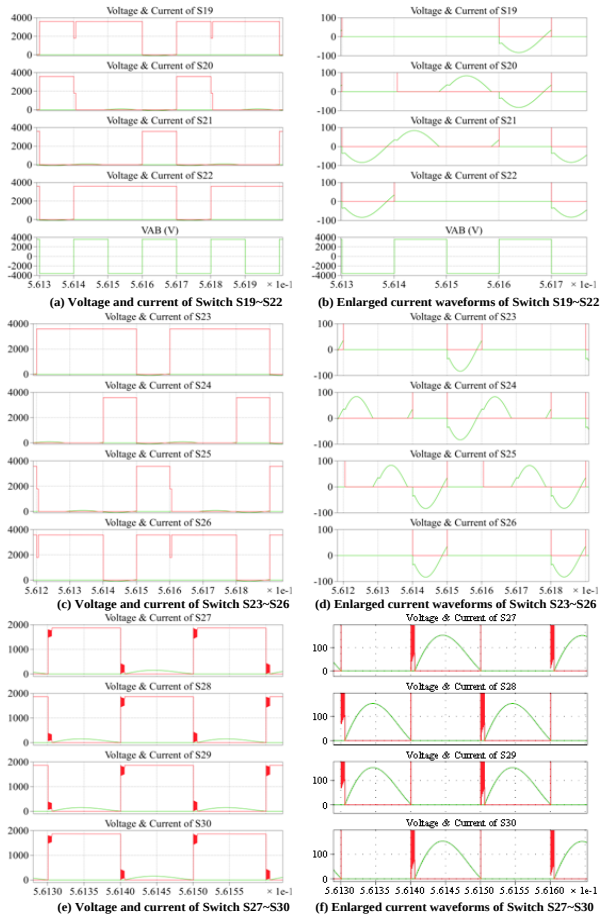

Fig. 14. Voltage and current waveforms of Switch S19~S30

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