Enhanced LVRT capability of Wind Turbine based on DFIG using Dynamic Voltage Restorer controlled by ADRC-based Feedback control

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Abstract. For grid-connected DFIG-based wind turbine, Fault Ride Through (FRT) or Low Voltage Ride Through (LVRT) capability is vital problem that need to be improved. This paper proposes an Active Disturbance Rejection Control (ADRC) strategy applied to Doubly Fed Induction Generator (DFIG) based Wind turbine (WT), which integrates a Dynamic Voltage Restorer (DVR). The DVR connect in series the DFIG output terminal and the utility grid. The ADRC scheme of the new topology DFIG-based WT with integrated DVR is designed to compensate grid voltage disturbances, which in turn meet LVRT requirement and increase the level of wind power penetration. The performance of this WT-DFIG-DVR structure is investigated in different operating scenarios in order to show the skills of the designed controllers.

1 Introduction

In recent years, renewable energy production has made great strides around the world to meet the challenge of drastic climate change and increasing demand for energy [1]. Among the various renewable energy sources, wind power is the fastest growing in the world [2,3]. In 2019, The 60.4 GW of new installations brings global cumulative wind power capacity up to 651 GW, and the Global Wind Energy Council (GWEC) predicts that more than 55 GW of new capacity will be added each year until in 2023 [1,4].

With the development of wind power, wind turbines (WTs) are widely used in electrical power systems. According to the speed control methods, WTs can be classified into four basic configurations: fixed-speed with squirrel cage induction generator (SCIG), ±10% of speed variation with wound rotor induction generator (WRIG), ±30% of speed variation with doubly fed induction generator (DFIG), and Full-variable-speed with SCIG, permanent magnet synchronous generator (PMSG), or wound rotor synchronous generator (WRSG) [5,6]. However, further development of this wind turbine topology is imperatively limited by Low Voltage Ride Through (LVRT) capability, which is dictated by most grid codes to operate under voltage sags at Point of common coupling (PCC) and remain connected to the grid to support voltage during and post-fault [7][8].

With a focus on the LVRT capability of DFIG-WTs, many countries have updated their Grid Code Requirements (GCR). For example, the German LVRT grid require that (1) The WTs must remain connected to
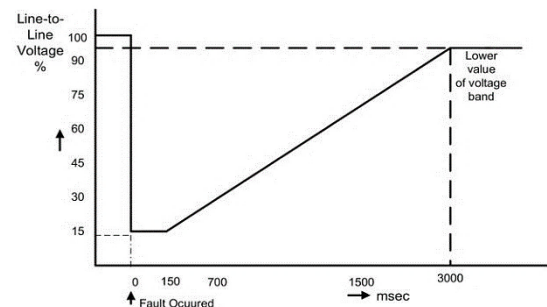

Fig. 1. Wind turbine German low-voltage ride-through (LVRT) grid criteria for voltage sags
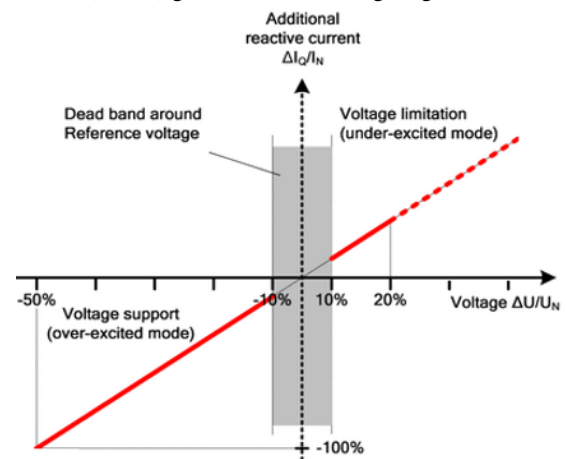

Fig. 2. Reactive power requirement as per E. ON grid code

the grid for at least 0.65 s after the fault appears, (2) the authorized fault voltage is 15% of its nominal voltage, and (3) voltage must return to 90% of its rated voltage within 3 s after fault clearance.

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According to the GCR for LVRT, WTs must have the ability to provide continuous operation during voltage sags, and the voltage should be maintained above the curve shown in Figure 2. In addition, reactive current injection during defaults is suggested by most GCRs. For voltage support, the E.ON requirement proposes that WTs should provide reactive current when the voltage reaches the dead band limit, and more reactive current injection is required when the voltage sags go further, as shown in figure 3 [1,8]. Support for reactive current in response to large voltage drops must be performed within 20 ms after fault detection [10].

DFIG-based WTs are mostly used and dominate the largest share of the market due to their advantages including wide speed range, independent control of real and reactive power, and lower power of the excitation converter [1-3,6]. In a DFIG-WTs as shown in Figure 3, the stator is directly connected to the grid while the rotor is connected to the utility grid via a Back-To-Back bidirectional converter (BTB). The RSC is controlled so as to master the active and reactive power supplied and also to capture the maximum wind power available. The GSC is used to keep the DC-link voltage constant, as well as to control the reactive power output and the active power exchanged between the rotor and the grid [3,6].

DFIG-based WT has been shown to exhibit problematic FRT behavior compared to other types of WT [1,7]. It suffers from great sensitivity to grid voltage sags or swells. During Voltage sags, damaging over-currents can flow in the DFIG stator and its rotor, an overshoot of the permissible DC-Link voltage threshold can be observed, and torque fluctuation can decrease the drive train lifetime [1,8]. To meet the LVRT requirement of GCR, the DFIG behavior during and after voltage sags must be examined as follows: (1) electromagnetic torques and turbines speed should be suitably controlled to ensure safe operation [1,8,11]; (2) overvoltage and overcurrent in rotor and stator windings should be limited to avoid damaging the BTB converters [10,11]; (3) voltage of DC-link must remain constant to ensure the desired operation of the GSC and RSC [1,8,12]; (4) sufficient reactive power is needed to support grid recovery [1-13].
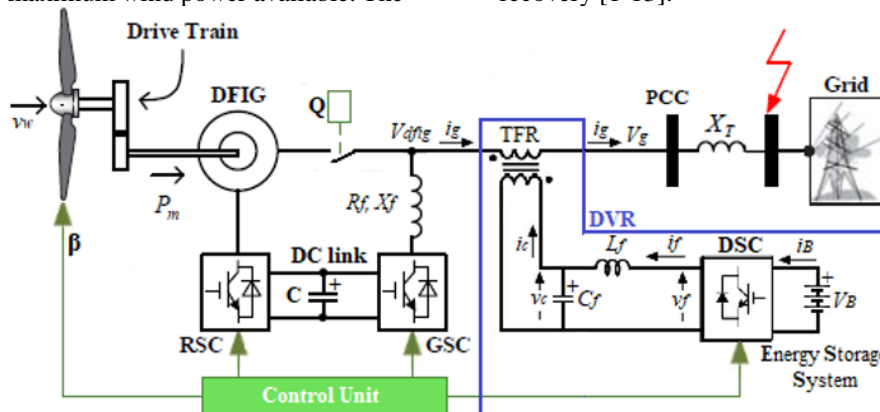

Fig. 3. Topology of Grid-connected DFIG-based WT with integrated DVR

In order to overcome these restrictions and subsequently enhance the LVRT capability of DFIG-WTs, Extensive methods including external retrofit techniques and internal control techniques have been proposed [1]. The internal control technique suggested in [1,12-15] can successfully overcome the most requirement of FRT capability. However, it will also complicate the control unit and will not be able to meet the strict grid code requirements alone. Although the hardware solution needs a costly investment, it has a good ability to deal with severe short circuit faults, and can also allow DFIG to tolerate large voltage sags [1,8,15].

Conventionally, shunt resistors known as crowbar are used to protect the rotor windings during the fault. However, its activation transforms the DFIG into a Squirrel Cage Induction Generator which necessitates a reactive power supply [8-13]. Thereafter DFIG can only inject reactive current after disconnecting the crowbar. The DC-Link chopper has shown its efficiency in limiting the DC overvoltage at its safety value, but it cannot help in the demagnetization of the DFIG after default [13,16]. Series dynamic braking resistors (SDBRs) and superconducting fault current limiters (SFCLs) are used as additional equipment to limit the inrush current undergone by the converters during transient conditions and to protect the rotor circuit against these transient overcurrents [17,18]. [7,10,15] prove that the DVR is capable of handling the transient fluctuations of a DFIG without need to other protective circuit during operation. The DVR is a competent voltage compensation device characterized by its fast response time as well as its better effect of restraining flicker [1,13,19].

Figure 3 shows the typical DVR topology connected to the DFIG. It consists of voltage source converter (VSC) for voltage synthesis, a coupling transformer, a DC energy source, and a harmonics filter. The purpose of the DVR system is to inject voltage to produce the desired stator voltage. Thus, the stator terminal is maintained at rated voltage at all times under normal and mains fault conditions. Therefore, the transient of DFIG current and power does not occur even if grid faults occur [15,20].

The efficiency of overcoming most network faults is the main criterion in choosing the right control strategy for controlling DVRs for FRT capability in DFIG-WTs. The DVR control unit is carried out in some stages and this includes voltage detection, generation of reference, control voltage application, and modulation generating the switching pulses for the VSI [15,21]. This control strategy is identified by feedforward open loop control [7,15,21-22]. Although this control scheme is simple

and guarantees stability, it has a poor transient regime and may have an imprecision (state error is not zero) in steady state [22-24]. In order to overcome these issues feedback controllers are used [15,25-26]. It consists of two; the first determines the reference compensation voltages, and the second regulates the output compensation voltages. This controller processes the measured output voltage of the DVR (or load voltage) to generate the VSI control output.

Due to PI regulator is not a suitable when its reference is time-varying, and the transfer function of the inverter is quite nonlinear. This paper uses DVR with feedback control using active disturbance rejection strategy (ADRC) [3,8] based voltage control. The enhancement of FRT capability in wind turbine based on DFIG using this ADRC-Feedback based DVR control is discussed for symmetrical fault conditions.

The remainder of this paper is organized as follows. Section 2 presents the DFIG modeling and its control part. Then, in section 3, the control scheme of DVR is designed. Simulations results are discussed in Section 4, and conclusions are drawn in Section 5.

2 Modeling of the typical DFIG-based WT with DVR

The proposed WT generator is composed of two parts: the DFIG and the DVR, as shown in Figure 3. The DVR is connected in series to the DFIG-WTG terminal. The modeling of each component is described below.

2.1 DFIG-WT

The typical model of DFIG is exposed in Figure 4. In dq-reference frame, the stator and rotor voltage vectors are defined in per unit by [3,8]:

$$V_{sdq} = R_s I_{sdq} + \frac{d}{dt}\psi_{sdq} + j\omega_s\psi_{sdq} \quad (1)$$

$$V_{rdq} = R_r I_{rdq} + \frac{d}{dt}\psi_{rdq} + j\omega_r\psi_{rdq} \quad (2)$$

Where V, Ψ, I, R, and ω represent respectively voltage, flux, current, windings resistance, and pulsation. The subscripts s, r, dq and indicate stator, rotor, dq-axis, respectively.
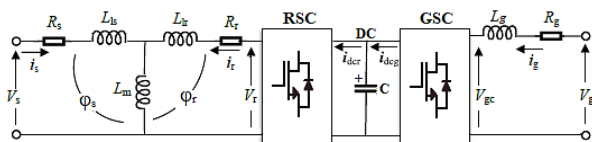

Fig. 4. The Basic Model of the DFIG

In addition, the stator and the rotor flux vectors are described by:

$$\psi_{sdq} = L_s I_{sdq} + L_m I_{rdq} \quad (3)$$
$$\psi_{rdq} = L_r I_{rdq} + L_m I_{sdq} \quad (4)$$

Where L_s and L_r are the stator and rotor self-inductances, respectively. L_m is the magnetizing inductance.

The stator powers are defined as follows:

$$S_s = 1.5\big(V_{sdq}I_{sdq}^*\big) = P_s + jQ_s \quad (5)$$

Where S_s, P_s, Q_s, and * are apparent, active, reactive, powers and complex conjugate.

The substitution of (3) and (4) in (2) gives the rotor currents dynamics as follows:

$$\frac{di_{rdq}}{dt} = -\frac{R_r}{\sigma L_r}i_{rdq} - \frac{L_m}{\sigma L_r L_s}\frac{d\psi_{sdq}}{dt} - j\omega_r i_{rdq}$$
$$- j\omega_r\frac{L_m}{\sigma L_r L_s}\psi_{sdq} + \frac{V_{rdq}}{\sigma L_r} \quad (6)$$

Where: $\sigma = 1 - \frac{L_m^2}{L_r L_s}$ is the DFIG dispersion coefficient.

Likewise, the harmonic filter currents and of the DC-link voltage are expressed by:

$$\frac{di_{gdq}}{dt} = -\frac{R_g}{L_g}i_{gdq} + \frac{1}{L_g}v_{gdq} + j\omega_s i_{gdq}$$
$$- \frac{1}{L_f}v_{gcdq} \quad (7)$$

$$\frac{C}{2}\frac{d\gamma}{dt} = 1.5v_{g,q}i_{g,q} - p_r \quad (8)$$

Where p_r is the active power in the rotor, and $\gamma = u_{DC}^2$.

2.2 Dynamic Voltage restorer (DVR)

The DVR in figure 3 is a voltage source converter (VSC) connected in series with the power line of the DGIG-WT terminal via three single-phase ideal transformers to quickly compensate for deteriorated grid voltages. The energy storage system (ESS) supplies the energy necessary to compensate the voltage sags. Another important DVR component is the LC filter which rejects the harmonics of the voltage synthesized by the DVR-VSC.

2.2.1 DVR Side converter (DSC)

The typical layout of a two-level VSC is shown in Figure 5(a). u_{fabc}, i_{fabc} are the three phase voltages and currents on the AC side of the DSC. In order to simplify the analysis, an average-value model of the two-level VSC, as shown in Figure 5(b), is used [7, 27-28]. Besides having almost identical low frequency dynamics and steady state with the detailed model, this model can greatly improve the simulation speed. In Figure 5(b), u_{fa}, u_{fb}, and u_{fc} are the three-phase components of the voltage u_{fabc} synthesized by the DSC. These three-phase components are expressed as a function of the ac voltage modulation indices ma, mb, and mc as follows [26-28].

$$v_{fi} = 0.5m_i V_B , i = a, b, c \quad (9)$$

Assuming the DSC is lossless, the power balance allows to write

$$i_B = 0.5\sum_{i=a}^{c} m_i i_{fi} \quad (10)$$

2.2.2 LC harmonic filter

The model of LC harmonic filter in figure 3 is described by the relationship between its input voltage (current) and that of its output as follows

$$\begin{cases} v_f = L_f \, {di_f}/{dt} + v_c \\ i_f = C_f \, {dv_c}/{dt} + i_c \end{cases} \quad (11)$$
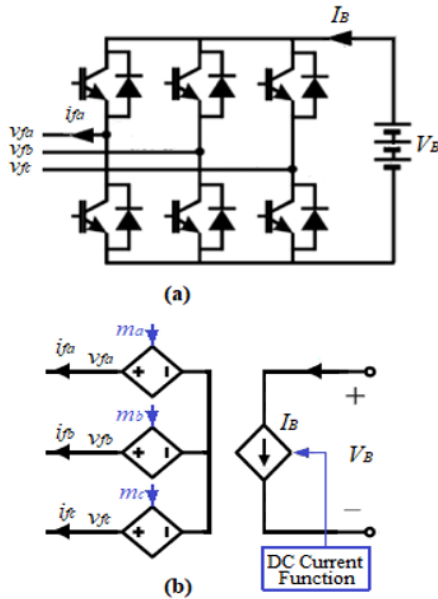
Fig. 5. 2-level VSC layout. (a) detailed model. (b) Average-value model

Where L_f, and C_f are the filter parameters. $v_f(i_f)$ and $v_c(i_c)$ are the voltage (current) synthetized by the DSC and the compensation voltage (current) respectively (see Figure 3).

2.2.3 Ideal Transformer

It is assumed that the TFR in Figure 3 is an ideal transformer. Then the relation between the voltage and the current of the primary and secondary sides is given respectively by:

$$\begin{cases} v_c = v_{dfig} - v_g \\ i_c = -i_g \end{cases} \quad (12)$$

Where the subscript *dfig*, *c*, and *g* indicate DFIG, DVR compensation, and utility grid respectively.

3 Control Scheme for DFIG-WT with DVR

From the general topology of the DFIG-based WT with DVR in Figure 3, three power conversion systems are used. These are Rotor Side Converter (RSC), Grid Side

Converter (GSC), and DVR Side Converter (DSC). The detailed control schemes for each converter will be designed in this section using the new active disturbance rejection control (ADRC) non-linear control strategy. The concept of ADRC and its application are detailed in [3,8].

3.1 Back-To-Back converters Control

The bidirectional BTB converter consists of the RSC, the DC link capacitor and the GSC. The main purpose of the GSC is to regulate the reactive power on the utility grid and to retain the DC-link voltage constant regardless of the direction and value of the rotor power flow. We assume that dc-link voltage U_{DC}, d-axis and q-axis grid converter currents (I_{gd}, and I_{gq}) are the state variables of the GSC controller. The control inputs of the GSC controller are V_{gcd}, V_{gcq}. Independent control of the active and reactive power can be achieved by the GSC current control in the d-q reference frame ($V_{gd}=0$, $V_{gq}=U_s$).

On the other side, the RSC controller is designed to control the stator active and reactive power outputs. Independent control can also be realized by controlling the rotor current in the d-q reference frame (the stator flux ψ_s aligns with the d-axis).

The control scheme of GSC and GSR with ADRC strategy is shown in Figure 6 [8].

3.2 DVR Side Converter Control

The purpose of the DVR is to quickly compensate for voltage disturbances of the grid and maintain the sinusoidal voltage injection profile. The operation of the control is synchronized with the supply voltage via the phase locked loop (PLL). In order to produce the PWM modulation signals, the control calculates the dq reference which is then converted to a three-phase stationary value [7,13,27-30]. Through the isolating transformer, the compensation voltages are injected to the utility grid at the point common coupling.

In Figure 7, based on dq-reference, the components of the d-axis and q-axis of v_{dfig}, v_g, v_c, and if are derived. DFIG voltage v_{dfig} is assumed to align with the q-axis,
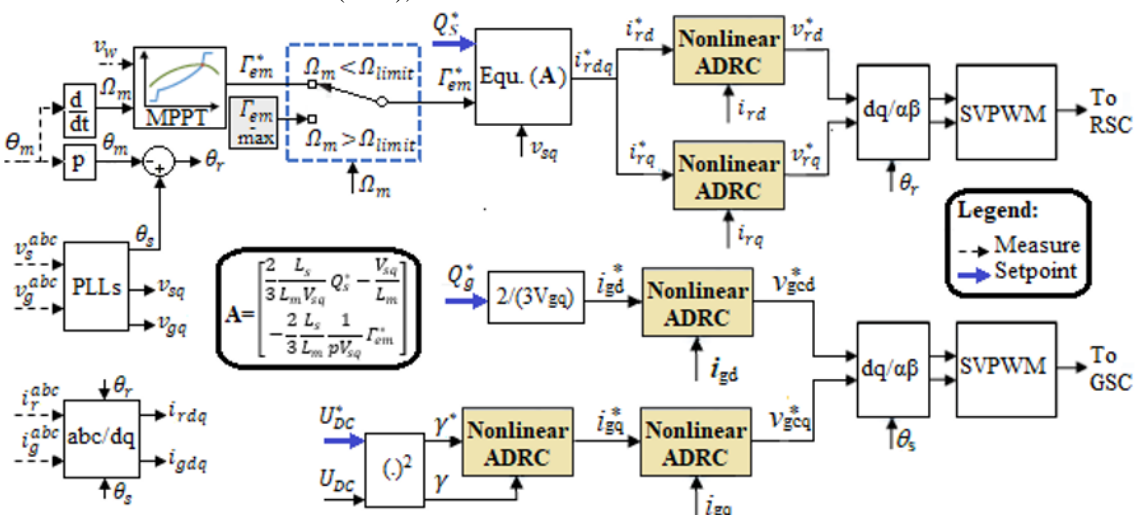

Fig. 6. Back-To-Back (RSC and GSC) Control scheme

i.e., $V_{dfig-d}=0$ and $V_{dfig-q}=U_0$ (pre-sag voltage). The DVR injected compensation voltages should be calculated carefully so that the voltages at DFIG terminal are properly compensated against the pre-sag voltages. The compensation voltage reference is expressed as follows:

$$V_{c-dq}^{Ref} = V_{dfig-dq}^{Ref} - V_{g-dq} \qquad (13)$$

Where $V_{dfig-dq}^{Ref}$ are the pre-sag DFIG voltages, V_{g-dq} are the grid voltage when the voltage sags occur.

In order to design the two DSC controllers using the ADRC strategy, the steps below are followed:

i- Equation (11) is written in the dq-axis frame as follows

$$\begin{cases} \dot{V}_{c-dq} = \dfrac{1}{C_f}I_{f-dq} - j\omega_s V_{c-dq} - \dfrac{1}{C_f}I_{c-dq} \\ \dot{I}_{f-dq} = \dfrac{1}{L_f}V_{f-dq} - j\omega_s I_{f-dq} - \dfrac{1}{L_f}V_{c-dq} \end{cases} \qquad (14)$$

ii- Equation (14) is written in the followed canonical ADRC form

$$\dot{x} = f(x,t,w) + bu \qquad (15)$$

Where the state vector has been chosen as $x = [V_{cd}, V_{cq}, I_{fd}, I_{fq}]^T$, the control input is $u = [I_{fd}, I_{fq}, V_{fd}, V_{fq}]^T$, $w = [w_1, w_2, w_3, w_4]^T$ is the vector of external disturbance, and the matrix of all disturbances f is given by:

$$f = \begin{bmatrix} \omega_s V_{cq} - \dfrac{I_{cd}}{C_f}\left(\dfrac{1}{C_f} - b_{11}\right)u_2 + w_1 \\ -\omega_s V_{cd} - \dfrac{I_{cq}}{C_f} + \left(\dfrac{1}{C_f} - b_{22}\right)u_2 + w_2 \\ \omega_s I_{fq} - \dfrac{V_{cd}}{L_f} - \left(\dfrac{1}{L_f} - b_{33}\right)u_3 + w_3 \\ -\omega_s I_{fd} - \dfrac{V_{cq}}{L_f} + \left(\dfrac{1}{L_f} - b_{44}\right)u_4 + w_4 \end{bmatrix} \qquad (16)$$

Where,

$$b = \begin{bmatrix} \dfrac{1}{C_f} & 0 & 0 & 0 \\ 0 & \dfrac{1}{C_f} & 0 & 0 \\ 0 & 0 & \dfrac{1}{L_f} & 0 \\ 0 & 0 & 0 & \dfrac{1}{L_f} \end{bmatrix} \qquad (17)$$

iii- For these four dynamics described by equations (14) - (17), the remaining steps of the ADRC strategy (development of Tracking Differentiator, Extended State Observer, and Nonlinear State Error Feedback F) presented in [8] will be easily applied.
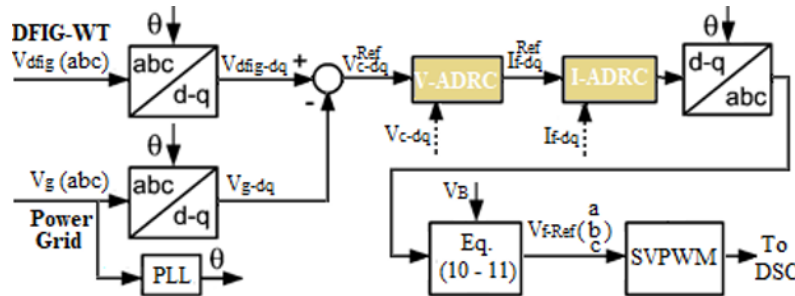

Fig. 7. Schematic diagram of the DSC controller

The control voltages issued by the second ADRC controller are transformed into a stationary abc reference frame transmitted to the modulator.

4 Simulation Results and Analysis

DFIG-based WT with DVR previously designed is simulated in MATLAB-Simulink environment as shown in Figure 8 and Figure 9. The simulation parameters of the DFIG and DVR are presented in Table 1.

In order to test the performance of the system designed to meet FRT capability requirements, two typical scenarios are simulated under voltage symmetrical fault operation of the utility grid. The first one investigates the FRT performances of DFIG-WT for symmetrical voltage sag of 35% of rated voltage which lasts 7.5 cycles between 0.5 s to 0.65 s. The second one studies the behavior of the DFIG-WT with respect to the occurrence of a short circuit lasting 150ms on the utility grid. These tests are established under a wind speed of 10 m / s assumed constant and the grid disturbance is too short to produce its noticeable variation. Furthermore,

the active and reactive power produced are 0.6 pu and 0 pu respectively.
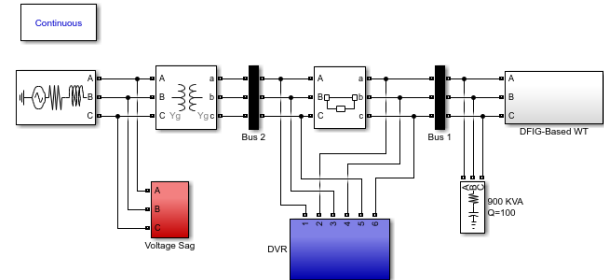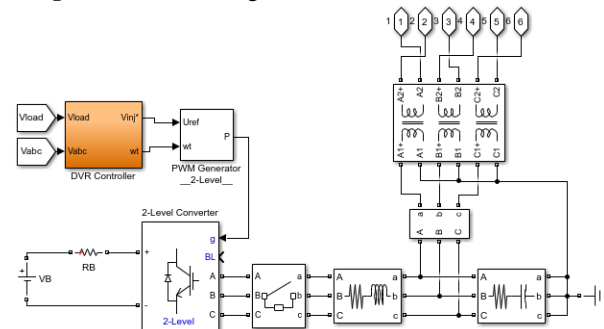

Fig. 8. Simulated Diagram of DFIG-based WT with DVR

Fig. 9. Simulated DVR structure

4.1 Test 1: Supply voltage with 0.35 symmetrical sag

The performance of the DFIG-Based WT with integrated DVR in the event of a 35% symmetrical voltage sag is given in Fig. 10 and Fig. 11. Fig. 10 (a) shows a symmetrical voltage disturbance lasting 150 ms from the moment 0.5 s which occurs in the utility grid. The DVR quickly (in less than 15 ms) produces the compensation voltage as shown in Figure 10 (b).

Table 1. DFIG-Based WT with DVR Parameters [3,13]

Component		Nominal value of quantities
DFIG-based WT	Turbine	R=43,36 m, C_{popT}=0,435, λ_{optT}=0,435, H=5,8 s
	DFIG	P_m=3 MW, f=50 Hz, p=2, n_{MAX}=1850 rpm R_s =27.285 mΩ, R_r=21.264 mΩ, L_{ls}=1.785 mH, L_{lr}=1.607 mH, L_m=15.168 mH
	3φ grid, DC link, harmonic filter	$V_{g,ll}$=690 V, R_g=1.59 mΩ, L_g=0.084 mH U_{DC}=1220 V, C=66.878 mF
DVR	ESS	V_B=1200, R_B=0.1Ω, P_B=3MW
	Filter	L_f=0.3 mH, C_f=10 µF
	Transformer	S_T=3MVA, ratio=1
Base value		S_{Base}=3 MVA, V_{Base}=398,4 V, ω_{Base}=314,159 rd / s

Hence, the DFIG terminal voltage is almost unchanged as shown in Figure 10 (c). the effect of this voltage kept constant on the typical DFIG-WT quantities is presented in Fig. 11. WT generator continues its production of active and reactive power as before the disturbance occurrence with a slight variation during the fault as illustrated in Fig. 11 (a). Fig11 (b) and Fig. 11 (c) show that the amplitude of currents at the stator and rotor are below the threshold of 2 pu prescribed by the criteria regarding the LVRT requirements. In Fig. 11 (d), the voltage of the DC-link maintains its constant value and its variation is very far from the threshold of 1.35$U_{DC-rated}$ tolerated by the criteria of the grid codes during voltage sags.
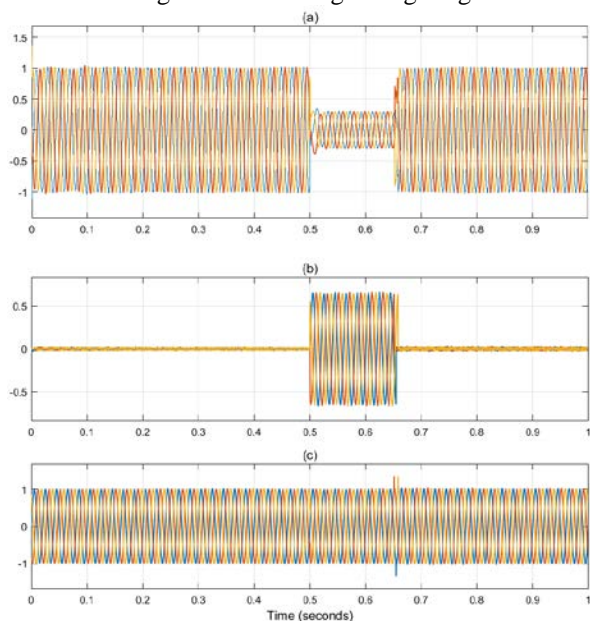

Fig. 10. Symmetrical grid fault with 35% voltage sag. (a) Grid voltage. (b) DVR Compensation voltage. (c) DFIG terminal voltage.

The behavior of the mechanical part is illustrated in Fig. 11 (e) where the DFIG speed is almost insensitive to the disturbance, while on the shape of the electromagnetic torque oscillations are observed during the appearance and clearance of the fault but their maximum amplitude is well below the limit 2 - 2.5 pu dictated by the LVRT grid code.

These simulation results show that the DVR controlled by the ADRC strategy effectively prevents the DFIG-based WT from experiencing transient voltages and currents and subsequently remains connected to the grid during the 35% voltage sag.
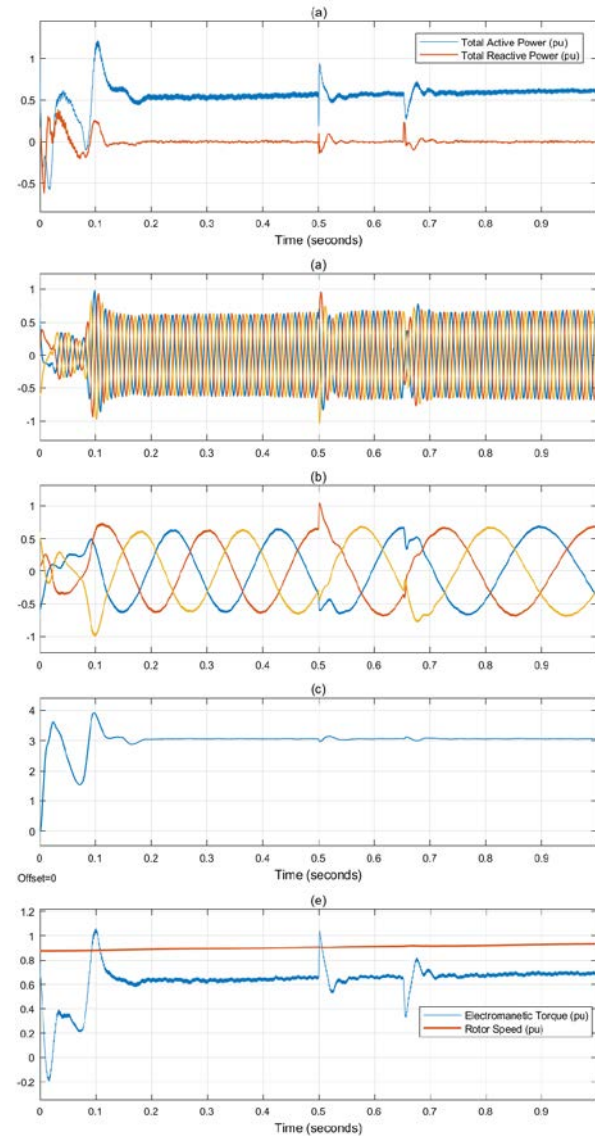

Fig. 11. (a) Active Power and Reactive Power of DFIG in pu. (b) DFIG three-phase stator currents in pu. (c) DFIG three-phase rotor currents in pu (d) DC-link voltage in pu. (e) Rotor Speed and Electromagnetic Torque of DFIG in pu.

4.2 Test 2: Supply voltage with 0.95 symmetrical sag

In this test, the scenario near the short-circuit with a voltage drop of 95% is simulated. The dynamics of the system are similar to the earlier test with a 35% voltage sag, as shown in Figure 12. The DVR promptly

compensates the voltage sag in Figure 12 (b) to reestablish the voltage at the DFIG-WT terminals as depicted in Figure 12 (c).
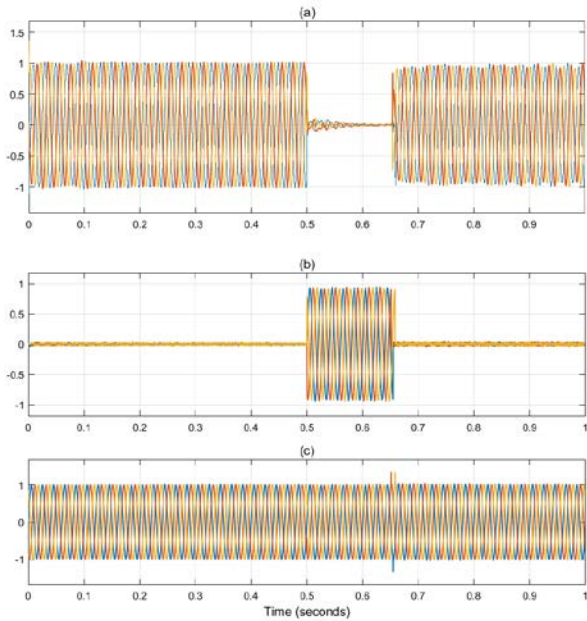

Fig. 12. Symmetrical grid fault with 95% voltage sag. (a) Grid voltage. (b) DVR Compensation voltage. (c) DFIG terminal voltage.

Figure 13 shows typical amounts of the WT generator which is subject to limitation by LVRT requirement in most grid codes of several countries in order to protect the WT generator but most importantly stay connected to the grid during the fault. Active-Reactive powers, DFIG currents in the rotor and the stator, DC-link voltage, and the mechanical quantities are presented in Figure 13 (a) to Figure 13 (e) respectively. Oscillations are observed over all of these sizes, in particular during the appearance of the fault and also during its disappearance. Despite the amplitude of these oscillations is greater than those of the previous test, it is well below the limits prescribed in the grid codes concerning the LVRT capability of WT generators. Based on the simulation results of this test, we deduce that the fast compensation voltage synthesized by the DVR makes a better contribution to stabilize the DFIG-based WT.

In order to conclude this section, the performance of DFIG-based WT with DVR structure controlled by ADRC technique is investigated in two operating scenarios. Despite the difficulties of adjusting their parameters, the designed ADRC-controllers of DSC, GSC and RSC are able to control the system in normal operation but especially in the event of fault and thereafter enhanced the LVRT capability of the WT generator.

5 Conclusion

In this paper, a DFIG-based WT with integrated DVR is proposed. The system structure and its ADRC-based control scheme are designed. In order to investigate the system performance, simulation results under normal operating conditions and operating in the event of a
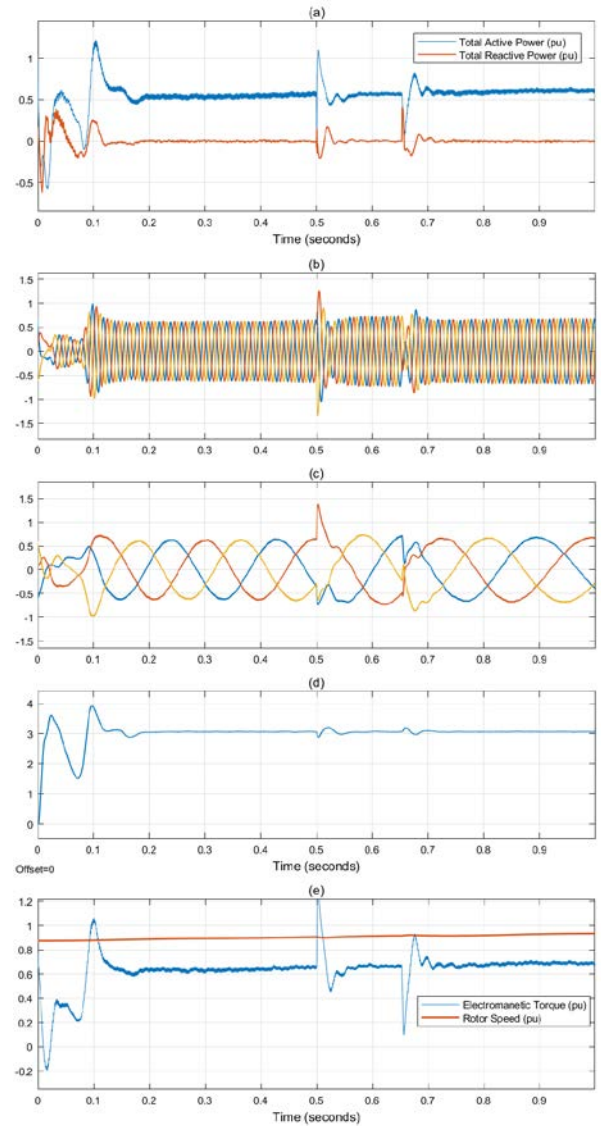

Fig. 13. (a) Active Power and Reactive Power of DFIG in pu. (b) DFIG three-phase stator currents in pu. (c) DFIG three-phase rotor currents in pu (d) DC-link voltage in pu. (e) Rotor Speed and Electromagnetic Torque of DFIG in pu.

voltage sag fault on the utility grid are presented. Using a DVR controlled by ADRC strategy can greatly enhance the LVRT capability of the DFIG-based WT under symmetrical voltage sag conditions. Despite its cost, DVR is highly recommended for already installed DFIG-WTs that do not have sufficient FRT capability.

In future work, comparative studies will be carried out with other controllers for the same structure and also with other LVRT improvement topology (Crowbar, Fault Currents Limiter, ...).

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