Design and simulation of frequency divider circuit based on multisim

Ling Li*, *Lingguo* Meng, and *Fuxun* Wang

School of Microelectronics, Shandong University, China

Keywords: multisim, frequency divide, design, simulator.

Abstract. Frequency divider circuit is the basic circuit in digital logic circuit. The circuit function is to divide or drop the frequency of the high frequency signal to get the lower frequency signal for a given frequency signal by division. On the Multisim software platform, using different design methods, as the foundation of middle scale integration chip 74LS161, design even frequency divider, odd frequency divider circuit and (N- 0.5) frequency divider circuit respectively. Each circuit design principle and method is illustrated and simulated. The results showed that the design is correct and conform to the proposed requirement. Experimental teaching applications based on Multisim software can improve design efficiency and reduce development time of design systems.

1 Introduction

NI Multisim simulation software is a convenient and powerful Electronic circuit simulation platform, whose predecessor is EWB (Electronic Workbench) software. It has become a virtual simulation auxiliary platform for teaching and experiment of Electronic professional courses in college and university, and has been widely used in Circuit Analysis, Analog Circuit, Digital Circuit, High Frequency Circuit and other courses [1-8].The software is equipped with a good deal of database simulation models of original components provided by semiconductor manufacturers, and contains more than 20 kinds of virtual instrument tests, such as oscilloscope, multimeter and other common instruments in the laboratory, which provides abundant convenient conditions for efficient and accurate simulation. The software interface is intuitive, easy to operate, design simulation analysis function is powerful. So Multisim simulation software is a powerful assistant teaching tool in the course of electronic circuit. The frequency divider circuit is a kind of circuit widely used in the digital system. Its function is to divide and drop the frequency of the high frequency signal to get the lower frequency signal. The low frequency signal can be used in the clock signal, the selected communication signal and the interrupt signal. Frequency divider circuit is mentioned in digital circuit course [9], and will be used for many times in later professional courses. The design of frequency divider circuit based on Verilog HDL hardware description language is mostly explained in the reference [10-12], but the design of frequency divider circuit based

* Corresponding author: liling.id@sdu.edu.cn

on 74LS series chips is rarely mentioned in the literature. To let the students in learning digital circuit more deeply understand the concept of frequency divider and the corresponding theory knowledge, in this work, through the Multisim simulation software platform, using the 74LS series of small and medium scale integrated circuit chip design simulation of various types of frequency divider circuit, can broaden the students' design ideas, exercise the logical thinking ability, to improve the comprehensive design of digital system, and to lay a foundation for the next course.

The nature of the frequency divider circuit is the integrated application of the counter circuit. The frequency divider coefficient $N=f_{in}/f_{out}$, in which f_{in} and f_{out} are the frequencies of the input and output signals respectively. Generally, according to the difference of frequency division coefficient, it can be divided into even frequency division, odd frequency division and decimal frequency division, etc. [13].Different types of frequency division coefficients correspond to different circuit structure designs. In this work, based on the midscale 4-bit binary counter chip 74LS161, combined with other logic control circuits, on Multisim software platform, the design principle and structure of even frequency divider, odd frequency divider and decimal frequency divider are described in detail, and the design results are verified by oscilloscope simulation.

2 Design and simulation of even-numbered frequency divider

The even-numbered frequency divider refers to the frequency divider coefficient N=2n (n= 1, 2...). This type of divider is easy to achieve a 50% duty ratio mode. The even frequency divider includes 2^n even frequency divider and ordinary even frequency divider respectively. To design different types of frequency dividers, different circuit design methods should be adopted according to the requirements and combined with the circuit function characteristics.

2.1 Design and simulation of 2^n even frequency divider

2^n even type frequency divider, that is, the frequency divider coefficient $N=2^n$, this type of frequency divider can directly put the corresponding output end of the binary counter into the frequency divider output signal end, without adding other logical control. Based on Multisim 14 virtual simulation software platform [14], the circuit design and simulation of 2^1, 2^2 and 2^3 frequency division are shown in Figure 1 and Figure 2 respectively. The chip 74LS161 is a 4-bit binary counter midscale chip with synchronous pre-set number and asynchronous reset function. As shown in Figure 1, the input control terminal of the circuit, ENP, ENT, ~ LOAD and ~CLR are connected to high-level VDD, and the circuit is in the normal counting function. Pre-set terminal A, B, C, D are connected to low level, pre-set value is 0, the circuit counting range is binary 0000 ~ 1111, that is, decimal 0 ~ 15. Connect the clock driver CLK to the signal generator (XFG1) "+" end, and the signal generator (XFG1)"COM" end is grounded. Set the signal as a square wave signal with a frequency of 1 kHz and an amplitude of 10 V. The output QA, QB, QC, are connected to the four channel oscilloscope A, B, C, while the wire colour is purple, green, and blue, respectively. CLK signal generator outputs pulse signal with oscilloscope D end, adjust the four channel oscilloscope signal A, B, C, D Y (pos.) value. As shown in figure 2, the simulation results of 2^1, 2^2 and 2^3 frequency division are correctly, and the cursor in the range from 1 to 2, the output frequency are respectively the input clock signal CLK of 2^1, 2^2, and 2^3 frequency divider.

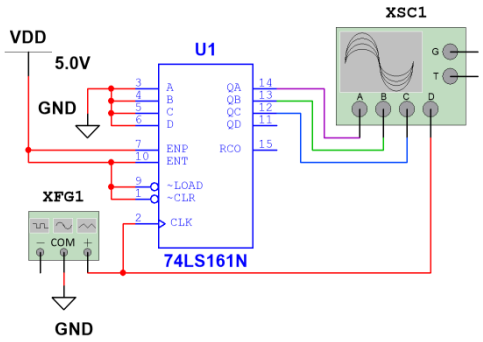

Fig. 1. 2^1, 2^2 and 2^3 frequency divider circuit design.

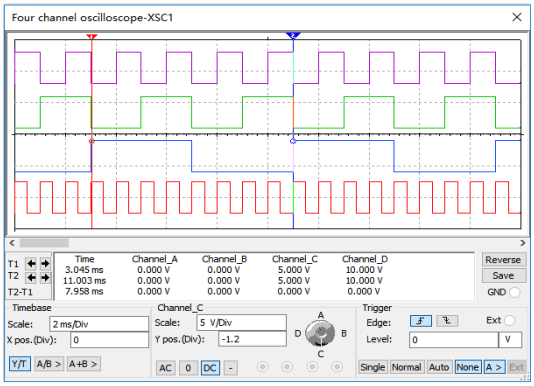

Fig. 2. Simulation results of 2^1, 2^2 and 2^3 frequency divider.

2.2 Design and simulation of common even frequency divider

The frequency division coefficient of the ordinary even type is even but $N \neq 2^n$. To design this type frequency divider circuit, first design MOD-N counter, then use the numerical comparator chip and counter output results (N/2) for comparison, to output high and low level signal. As an example, the circuit design and simulation of a frequency divider with a frequency divider coefficient of 10 is taken to illustrate the design and simulation result. As shown in figure 3, 74 LS161 chip, the control input end, such as ENP, ENT, ~ CLR are connect with high level, and using its sync function. When the circuit output QD, QC, QB, QA for 1001, the number of sync control end (to the ~LOAD) on the next CLK pulse comes to low level will pre-set number A, B, C, D, the pre-set number is "0000" in counter, the circuit is set to modulus of 10, counting circuit range is 0000 ~ 1001.

Counter output QD, QC, QB, QA respectively with that of the numerical comparator chip 74LS85 input end, A3, A2 and A1, A0,respectively. B3, B2, B1, B0 of 74LS85 chips are set with value number “0101” (decimal Numbers 5, N / 2, N = 10). When the counter 74LS161 chip output of 0 ~ 4, the comparator chip 74LS85 output OAGTB is 0, when the counter output is 5 ~ 9, the output is 1. The frequency circuit of the output signal duty ratio is 50%. Viewing the simulation results through the oscilloscope, as shown in Figure 4, it can be seen that the circuit design of 10 frequency division is correct.

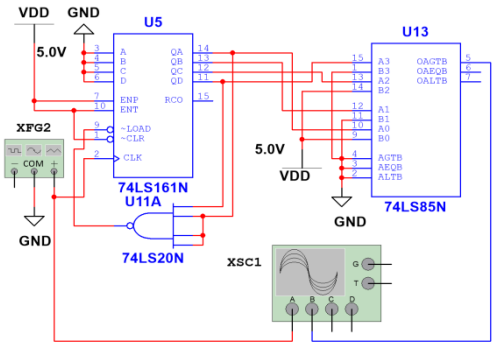

Fig. 3. 10 Frequency division circuit design.

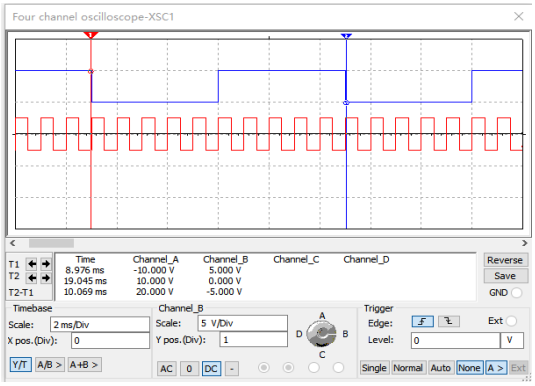

Fig. 4. 10 frequency divider circuit simulation result.

3 Design and simulation of odd frequency divider

The frequency division coefficient of the odd type divider is odd, that is, the frequency division coefficient is N=2n+1 (n= 1, 2...).Odd type frequency divider, in order to ensure the design result is 50% duty ratio of the waveform frequency division, need to use up and down edge the trigger design respectively, to design two N a binary counter, and counter output compared with the comparator chip, produce((1/2 + N/2) / (N/2 +1/2))×100% duty ratio output logic , and then put the two output logic AND operation, finally produce the duty ratio for 50% of the odd type design of the divider. The circuit design of a frequency divider with a frequency divider coefficient of 5 is taken as an example. As shown in figure 5, the 74LS161 (U1) is designed with rising edge counter of MOD-5, and by 74LS85(U2) comparator chip, designed the duty ratio for 60% of the frequency divider. Analogically, the falling edge counter of MOD-5 is designed as shown 74LS161 (U3) and 74LS85 (U10) with the duty ratio for 60%. And then put the two counter output by using the AND logic. As shown in figure 6, by four channel oscilloscope waveform simulation results waveform (red) as the input clock signal, as shown with waveform A. The waveform B (green) is the rising edge MOD-5 counter output, as the duty ratio of 60%, while the waveform C (purple) is the falling edge MOD-5 counter output, as the duty ratio of 60%. The waveform D (blue) is 5 frequency divider with duty ratio of 50% outputs waveform simulation results, and the result is correct.

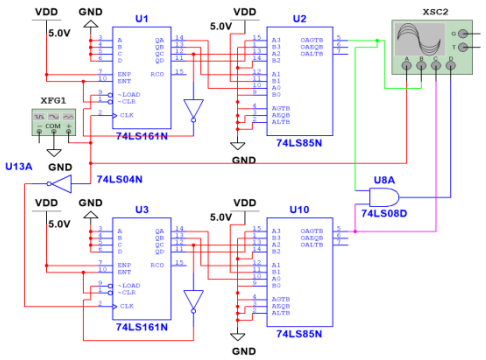

Fig. 5. 5 Frequency division circuit design.

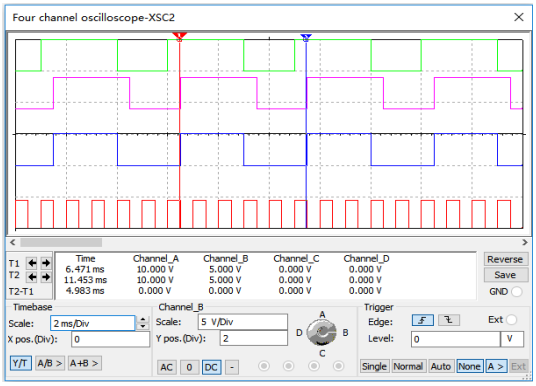

Fig. 6. 5 frequency divider circuit simulation results.

4 Design and simulation of (N-0.5) decimal frequency divider

(N-0.5) Decimal type frequency divider is a kind of decimal type frequency divider. The design of this type of frequency divider includes three main parts: MOD-N counter design, binary frequency circuit design and XOR logic. The principle and design method of (N-0.5) fractional frequency divider are illustrated with the example of 3.5 frequency divider circuit. Figure 7 and Figure 8 are the circuit design and simulation verification results of 3.5 frequency divider respectively. As shown in figure 7, module 1 (as shown in figure in the yellow box, similarly hereinafter) for chip 74LS161 constitute MOD-4 (N = 4, 4-0.5 = 3.5) counter, module 2 constitute MOD-2 counter circuit, module 3 is XOR logic.

The input end of XOR logic (U10A) is the QA signal of module 2(U11) and the standard pulse signal output by the signal generator (XFG2). The output of XOR logic is the clock input signal CLK of MOD-4 counter in module 1. As shown in figure 8, 3.5 frequency divider circuit simulation results, the waveform for standard pulse signal generator, waveform A(red), set as the bottom in the oscilloscope waveform. The waveform B (green) is MOD-4 counter clock input (that is, the module 3 XOR logic output), as the top waveform in the oscilloscope waveform. After XOR logic, the square wave signal waveform is not standard. Waveform C (purple) is the MOD-4 counter output signal, according to the output cycle is 3.5 times that of the original clock, and the duty ratio with the output waveform is (1.5/3.5 = 43%) , and is not a standard square wave signal, as shown in figure 8. The waveform D (blue) represents the frequency division output of the module 2 circuit, generating an XOR logic input signal. The QB output cycle of circuit module 1 (U8) is 3.5 times of the original clock, so as to

realize the output signal of 3.5 frequency division of the input original clock. The simulation results show that the circuit design of 3.5 frequency division is correct.

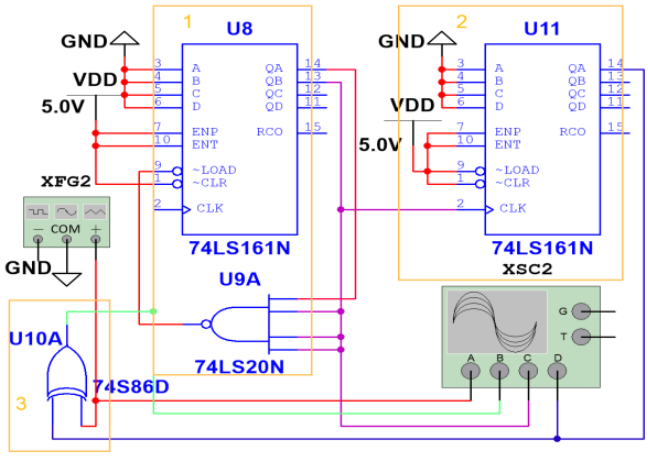

Fig. 7. 3.5 Frequency division circuit design.

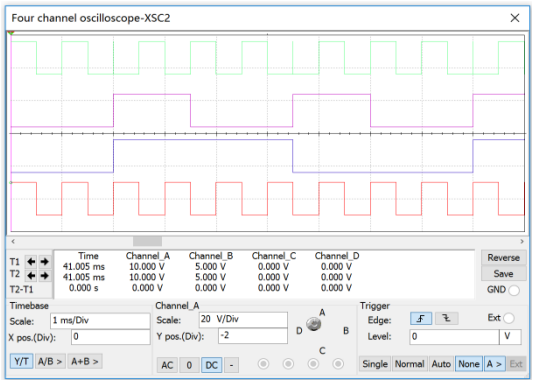

Fig. 8. 3.5 frequency divider circuit simulation results.

5 Conclusion

Multisim software is used to design even, odd and fractional frequency dividers for different frequency division modes. Full use of the software platform fast, efficient, intuitive characteristics of the circuit design and waveform simulation. Based on Multisim software platform as a hardware platform of virtual simulation experiment of complement each other, students can make full use of their spare time to fully prepare and practice curriculum design, improve the efficiency of practical courses, at the same time is helpful for students to a better understanding of the theoretical knowledge and comprehensive application system, fully arouse interest in learning, improve the effect of autonomous learning, in the face of complex electronic system design for the future, science and technology innovation ability lays the foundation, etc.

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