Functional units modelling of the controller for the energy-efficient power converters hardware

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Abstract. The functional units SPICE-models design steps of the controller K1156EU2 using Micro-Cap 12 computer assisted circuit design software. Presented methodology includes functional analysis of the units. Developed models are used as the baseline components for the controllers' SPICE-macromodel. The models and respective key characteristics are aligned with and represent fully all claimed hardware counterparts' specifications. Each model can be tuned through the respective set of parameters, hence enabling energy consumption characteristics optimization during the design phase.

1 Introduction

An important step of the energy-efficient power converter devices design (e.g., switching power supplies) is mathematical modeling using computer assisted circuit design software (PSpice, OrCAD, Micro-Cap, Multisim, etc.) [1, 2]. However, such design can be jeopardized due to the lack or limited number of available formal models of the controller units, particularly in case of locally sourced/built hardware components, e.g., integrated circuits (Russian Federation).

To ensure interoperability across the most of computer assisted circuit design software, the SPICE integrated circuits description language [3 - 6] is used for the models' design and development.

Typically, the macro model design is carried out in several steps. Initially, all operations are captured and formalized across the blocks of the functional diagram which describes all individual unit models. Next, all individual models are recombined into the final output including model attributes - the macromodel. The models design process is iterative; hence it can contain the model's quality assurance steps through the characteristics fine tuning [7].

2 Controller K1156EU2 functional design

The design of the macromodel is done according to the functional diagram of the controller K1156EU2, shown in Figure 1 [8].

K1156EU2 integrated circuit is designed to control pulsed secondary power supplies with frequency ranges up to 1 MHz. The microcircuit provides the shortest signal travel

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time through the comparators and internal logic at the maximum bandwidth and slew rate of the error amplifier. The controller is compatible with voltage feedforward systems and is designed to operate in either voltage or current pulse width modulated (PWM) modes.

The architecture of the K1156EU2 controller is quite traditional [8]. The K1156EU2 circuit, in addition to the DA9-DA10 half-bridge output stage, includes a sawtooth voltage generator (oscillator), a DA1 bias source at 1.25V, a DA5 undervoltage blocking circuit, a reference voltage source (ION), a DA2 wideband error signal amplifier, a DA6 comparator , DD3 latch, DD5-DD6 phase splitter, VT1-VT2-DA7 soft start unit, DA3 current limiting and DA4 circuit shutdown comparators, DA8 reference voltage control comparator, DD8-DD9 output key control circuit [8].

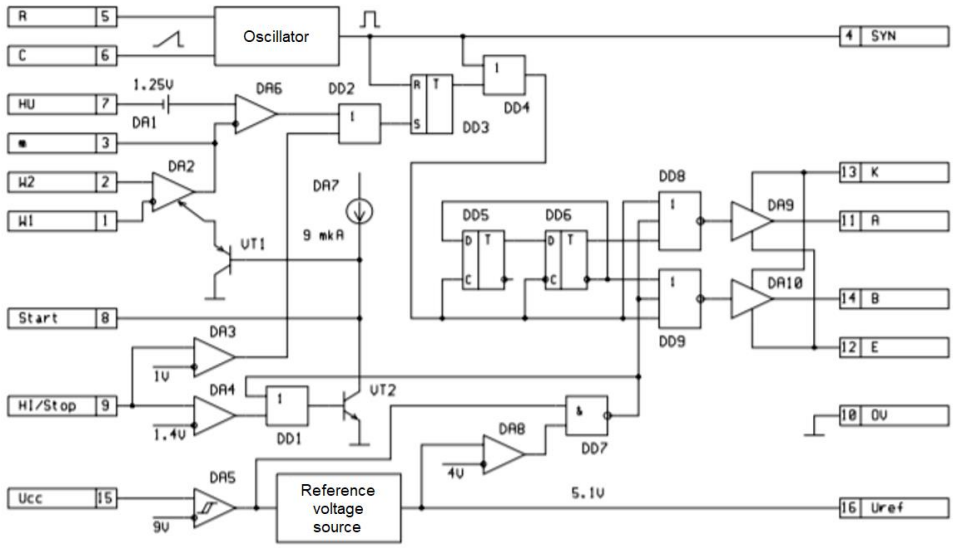

Fig. 1. Functional diagram of K1156EU2

When building a macromodel it is imperative to optimize both internal structure and functional units' parameters used for the internal IC logic implementation. Furthermore, the optimal model design of electronic devices should be based on optimal models design of the respective components and other integral parts. To clarify, the optimal models are defined as the formal entities with aligned characteristics and respective functions to their claimed hardware counterparts, with proven and guaranteed performance characteristics, with best computational performance and lowest overhead, hence ensuring high convergence of computational algorithms [7].

2.1 Oscillator

Master oscillator - is oscillator designed to operate at frequency ranges up to 1 MHz, determined by the parameters of the external RC-circuit. The SPICE model of the oscillator is shown in Figure 2. Resistor R is connected to a 3 V voltage source. The current source G1 generates the charge current of the capacitor C, which determines the front slope of the sawtooth pulse. The key S1 forms a fast-trailing edge of the pulse. Initially, the switch is open and does not affect the process of charging the capacitor. As soon as the voltage reaches 2.8 V, the key closes and the capacitor quickly discharges. When the voltage drops

to 1V, the key will open again, and the charging process will be repeated. Further, the generated pulses are converted into rectangular ones using a controlled voltage source E1.

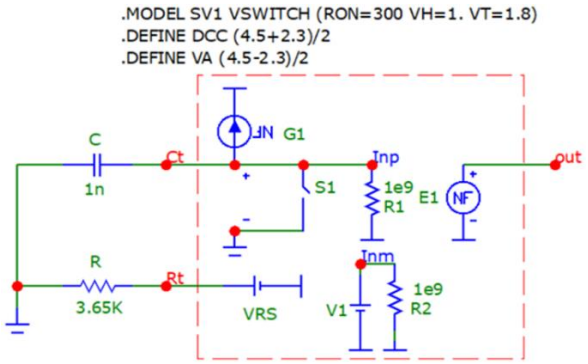

Fig. 2. Model of the oscillator

The timing diagrams of the operation of the oscillator model are shown in Figure 3. At the nominal values of the RC-circuit elements (R = 3.65 kOhm and C = 1nF) corresponding to the passport data of the K1156EU2 microcircuit [8], the pulse frequency of the model oscillator 397 kHz practically does not differ from the pulse frequency of the physical prototype (400 kHz +/- 10%)

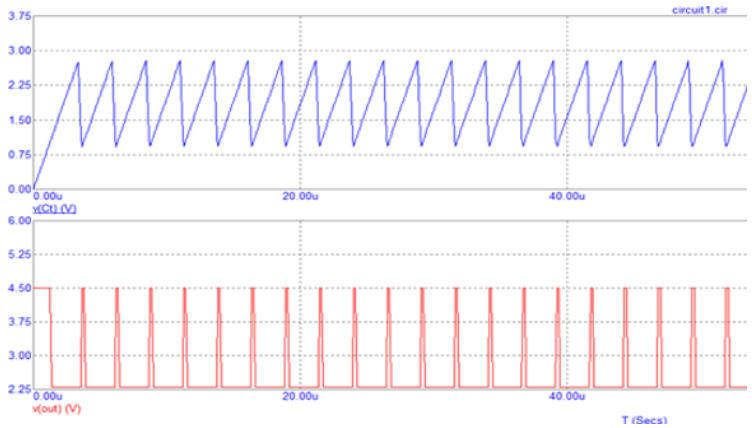

Fig. 3. Timing diagrams of the oscillator model

2.2 Error amplifier

The error amplifier in the K1156EU2 microcircuit is an operational amplifier with a wide bandwidth. The unity gain frequency is 5.5MHz. The slew rate of the output signal is not less than 12V / us. The voltage gain is 95 dB. The output voltage is high level 4 V, low level from 0 to 1 V.

ERRAMP element from the Micro-Cap software library is used as a model of the error amplifier. By changing the parameters Vhigh (upper limiting level), Vlow (lower limiting level), Pole (frequency of the 1st pole of the frequency response), GAIN (DC gain), you can achieve complete coincidence of the main characteristics of the amplifier with the reference data [8].

So, for the K1156EU2 microcircuit, according to the technical documentation, Vhigh = 4, Vlow = 0.1, Pole = 100, GAIN = 60000. The corresponding characteristics of the mismatch amplifier are shown in Figure 4.

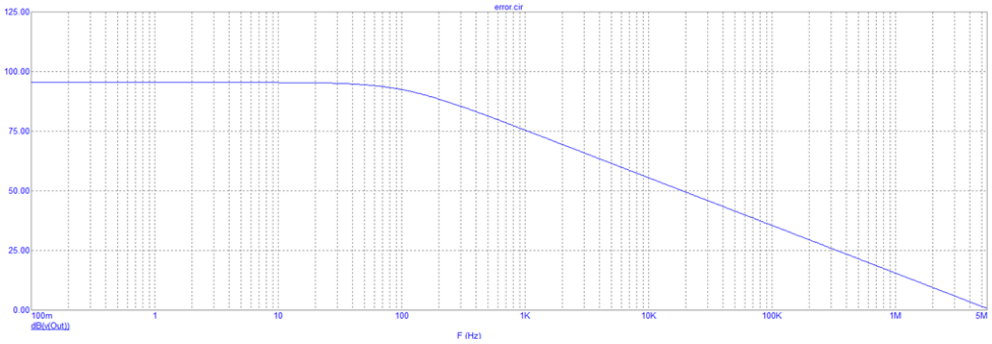

Fig. 4. Frequency response of the mismatch amplifier

As can be seen from Figure 4, the voltage gain is equal to 95 dB, and the unity gain frequency is 5.5 MHz, which corresponds to the parameters specified by the manufacturer of the K1156EU2 controller.

2.3 Reference voltage source and undervoltage protection

In the controller, the reference voltage source (RV) consists of a temperature-compensated 1.25 V voltage regulator and an amplifier DA1. The divider of the feedback signal R3 - R4 allows you to obtain the required output voltage (Figure 5).

In the K1156EU2 microcircuit, comparators, internal logic, a 1.25 V bias source, an operational amplifier, and an oscillator are powered from the ION.

Before the ION, in the controller (see Figure 1) there is a protection circuit against undervoltage, and after that there is a comparator for controlling the value of the reference voltage. If the controller supply voltage is less than 9.2 V, then the DA8 undervoltage protection comparator is triggered. In this case, a logical 0 at the output of the comparator, applied to the element DD7, will form a logical 1 at its output, which is fed to the control elements of the output keys DD8 and DD9. As a result, logical zeros will appear at the outputs of the keys, which corresponds to their off state.

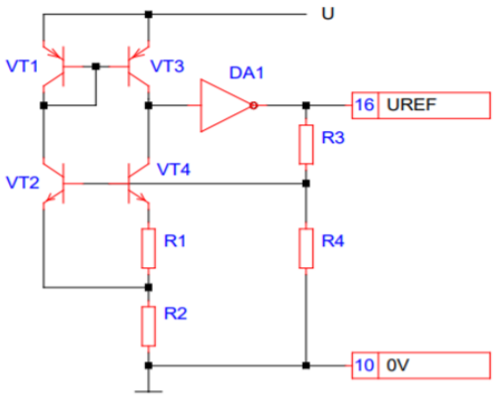

Fig. 5. Scheme of the reference voltage source

With an increase in the reference voltage more than 9.2 V, the undervoltage protection comparator forms a logic 1 at the output, which is fed to the DD7 element and the reference voltage source and opens the power switches and provides switching on power supply [8].

When the voltage at the REF output is less than 4 V, the reference voltage control circuit is triggered. At the output of the circuit, a logical 0 is formed, which, after element DD7, already in the form of a logical 1, turns off the power switches and the soft start circuit, and lowers the voltage at the output of DA8 (figure 1) to zero [8].

The SPICE model of the reference voltage source and undervoltage protection is shown in Figure 6. The model is implemented based on a comparator and Clipper function block (X4) taken from the Micro-Cap software library. When using the Clipper block, it is advisable not to add the REF undervoltage protection circuit, since if the supply voltage is greater than 9 V, the RON based on the Clipper block will be guaranteed to maintain 5.1 V. In this case, it makes no sense to add an extra comparator and complicate the model. Thus, instead of element DD7, the model uses an inverter.

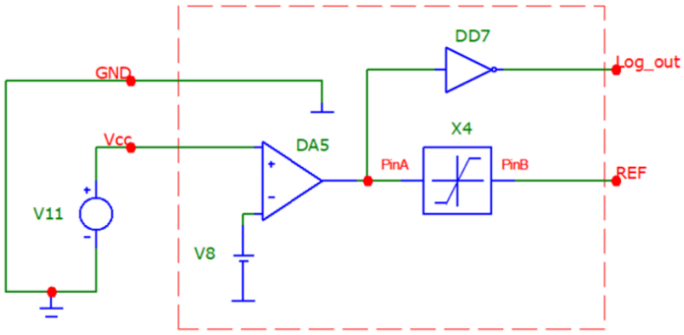

Fig. 6. Model of the reference voltage source and undervoltage protection

2.4 Comparators

As a comparator model, the standard model of an ideal comparator [10] is used, which is distinguished by simplicity and, accordingly, a higher speed of calculations than if the model was created directly according to the scheme described in the technical documentation of the controller.

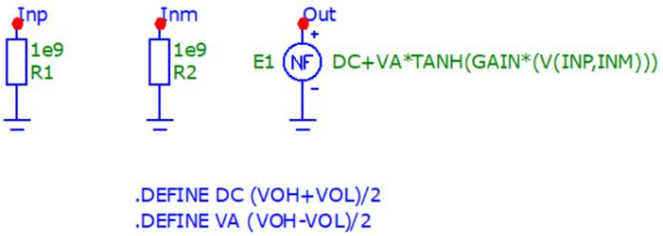

Fig. 7. Comparator model

2.5 Output drivers

The output half-bridge stages of the DA9, DA10 controller (see Figure 1) can switch a 1000pF load with a voltage of 15 V in 30 ns. The peak current value is not less than 1.5A.

The model of the output drivers is based on the driver model described in [7].

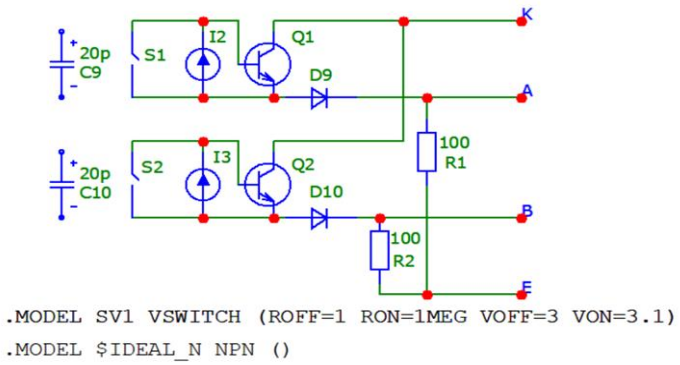

Fig. 8. Model of output drivers

Such a model is compatible with any circuit design software. The characteristics of the model of the output drivers are shown in Figure 9.

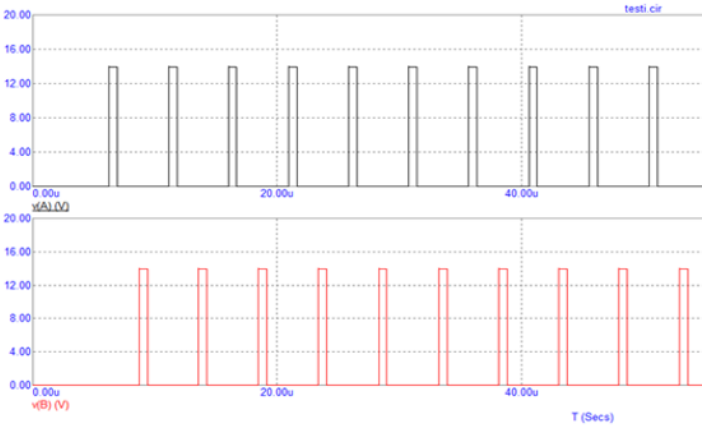

Fig. 9. Characteristics of the output drivers

2.6 Triggers and logic gates

The DD3 latch element is an RS flip-flop. Phase split triggers DD5 - DD6 are D-type triggers. Models, both triggers and logical elements OR (DD1, DD2, DD4), OR-NOT (DD8-DD9) and others are borrowed from the library of components of the Micro-Cap 12 software.

3 Conclusion

The functional units SPICE-models design steps of the controller K1156EU2, are based on integrated circuit structural analysis. Entire design allowed us to develop models with key

characteristics which are aligned with respective hardware counterparts' specifications. Each model can be tuned through the respective set of parameters, hence enabling energy consumption characteristics optimization during the design phase. All models presented can be used for the design and development for other than K1156EU2 macromodels with similar or shared architecture [11, 12].

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