Performance of 7-level cascade H-bridge multi level inverter driven induction motor drive

Suresh Kumar Tummala[1*], *Kyama* Hemalatha[1], *Ibrahim H.* Al-Kharsan[2,3], *Vijaylakshmi* Sajwan[4]

[1]EEE Department, Gokaraju Rangaraju Institute of Engineering and Technology, Hyderabad, INDIA
[2] Computer Technical Engineering Department, College of Technical Engineering, The Islamic University, Najaf, Iraq
[3] Department of Electrical Engineering, Faculty of Engineering, University of Kufa, Najaf, 54001, Iraq
[4] Uttaranchal School of Computing Sciences, Uttaranchal University, Dehradun 248007 INDIA

Abstract. In recent times, many of industrial applications require smooth control over a wide range of speeds or smooth torque control without effecting motor performance and efficiency. So, cascaded H-Bridge multilevel inverters convert the low or medium level voltage to medium or high level of output voltages. In this paper, a cascaded H-Bridge multilevel seven level inverter is operated by using sinusoidal pulse width modulation technique. This PWM technique will improves the smoothness of waveform by reducing the lower order harmonics. And analysed its performances like speed, torque, THD etc.

Keywords :- CHB MLI- cascade H-bridge multi-level inverter, SPWM- Sinusoidal pulse width modulation, THD- Total harmonic distortion, PD – Phase disposition, POD – Phase opposition, APOD – Alternate phase opposition disposition, PSPWM – Phase shift PWM, COPWM- Carrier over lapping PWM, MCSPWMVF – Multi carrier sinusoidal pulse width modulation with variable frequency.

1 Introduction

The induction motor is the most often used electrical machine in virtually all simple, medium, and high voltage industrial engineering processes since it is less costly and has a greater dependability. Because of the recent development of high power demand and low cost power electrical equipment [1], drives now have a broader variety of applications. As a result, induction motor drives and other ac drives, together with power electronic converters, have replaced dc motor drives in industry. The most difficult obstacle [2] to installing AC drives

* Corresponding author: sureshkumar255@gmail.com

is selecting an adequate power electronic converter. The nonlinear dynamic performance of the induction motor, which includes extra nonlinearities in the converter dynamics [3] and switching performance, increases the bar for how difficult the control job is.
A multi-level inverter might successfully replace typical voltage source or current source inverters. Multilevel inverters provide several advantages, including reduced voltage stress, higher output voltage quality, and increased power rating [4]. Multilevel power converters are voltage generators that cascade numerous smaller discrete voltage levels to produce a large output voltage. Furthermore, multilayer inverters decrease voltage [5] stress between devices, have low output voltage dv/dt, little electromagnetic interference, and low total harmonic distortion (THD), and increased switching frequency increases motor performance [6]. As a result, they are becoming an attractive alternative to medium-voltage high-power ac drives.

For more than three decades, multilevel converters have been actively employed in the industrial sector and have been the subject of substantial research and development. Despite the fact that this technology is still in its early phases of research [7], various creative contributions and commercial topologies have lately been unveiled [8]. The schematic diagram of open-loop v/f control of IM with cascaded MLI utilising SPWM approach is shown below .1[96].

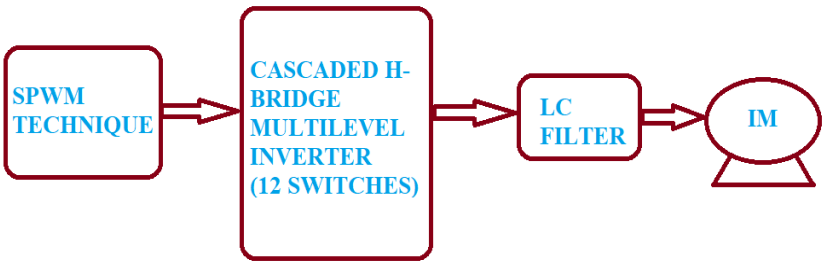


Fig.1 Block diagram approach for the proposed model.

Multilevel converter topologies have been categorized as

1.1 Diode clamped MLI

Neutral clamped MLI is another term for diode clamped MLI. When used with 3-level diode clamped MLI, it provides a mid-point or neutral point voltage [10]. The diodes will clamp the DC voltage into a variety of states in the AC output waveform. The key advantages are that it may be operated at a high switching frequency and that increasing the number of levels improves the harmonic content [12]. However, as the number of levels rises, greater voltage blocking capability diodes are required, as are high voltage rating switches and capacitor voltage imbalance [11].

1.2 Capacitor clamped MLI

The actual and reactive power will be regulated by this capacitor clamped MLI. It is also known as the fly-back capacitor MLI. The key distinction is that clamping diodes have been replaced by capacitors [2]. It features switching redundancy throughout the phase to balance the voltage of the flying capacitor [13]. Because it runs at a high switching frequency, switching losses will be greater.

1.3 Cascaded H-Bridge MLI

Switches are connected in such a way that it resembles an H-Bridge, a number of H-Bridges are connected in series, and each H-Bridge has a separate DC source, which is cascaded as shown in fig.2. As the H-Bridges are cascaded, the number of voltage levels increases, and it synthesises output waveform from several DC sources. [7].
The Single phase CHBMLI configuration is shown below in Fig.2. It is a cascaded seven level MLI [5].

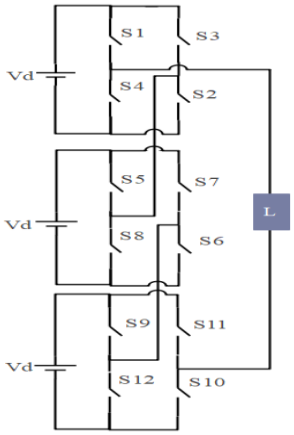


Fig.2 Configuration of CHBMLI

2 PWM Technique

A variety of modulation schemes based on switching frequency have been developed. Fundamental switching frequency PWM and high switching frequency PWM are the two types. Figure 3 depicts the classification of PWM approaches. This MLI employs sinusoidal PWM. At the same time that various multilevel inverter topologies are being presented, numerous modulation methods and control theories for the same have been developed, such as sinusoidal pulse width modulation (SPWM), space vector modulation (SVM), and selective harmonic elemination technique using a sinusoidal waveform [7].

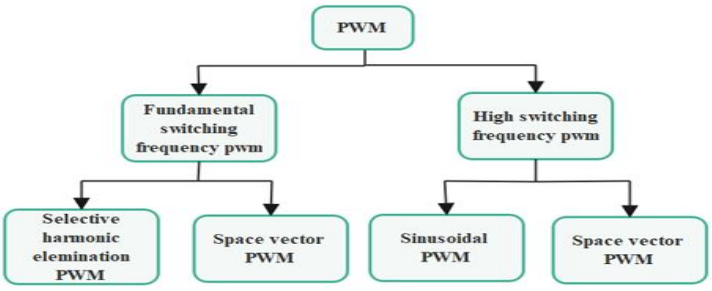


Fig.3. Categorization of PWM Techniques

2.1 Sinusoidal PWM

There are various approaches to achieve SPWM those are

2.1.1 Phase disposition PWM

A basic sinusoidal modulating signal is compared to all carrier signals with the same frequency, amplitude, and phase but a variable DC offset to occupy various levels in this manner. The intersections of the modulating signal and the related triangle signals are where the gating signals for the relevant level switches are generated. Because all carrier waves are picked with the same phase, the process is known as PD. The technique is depicted in Fig. 3, where the required number of triangular signals is indicated (n-1). Where n is the number of tiers. As seen in fig.4 [4].

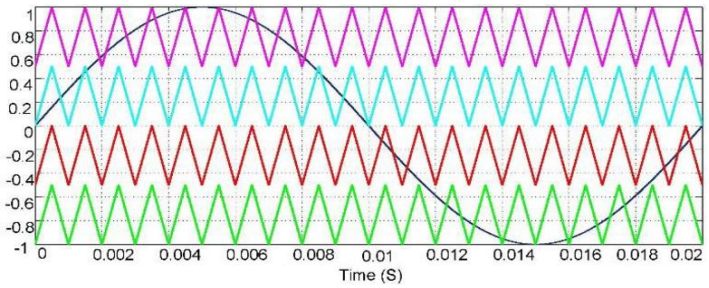


Fig.4. Phase disposition

2.1.2 Phase opposition disposition PWM

In this approach, the carrier signals above the reference zero voltage are 180 degrees out of phase with the carrier signals below the zero reference voltage, and it also includes carrier signals with the same frequency and amplitude but different in phase, as shown in fig.5. [4].

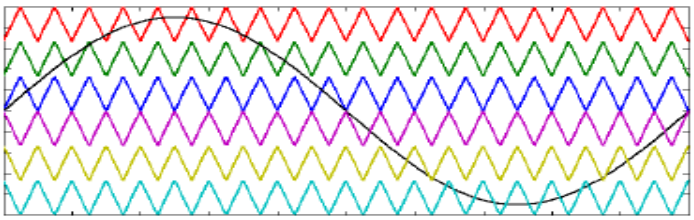


Fig.5. Phase opposition disposition PWM

2.1.3 Alternative phase opposition disposition PWM (APOD)

It employs carrier signals of the same frequency and amplitude, but each one is 180 degrees out of phase with the one next to it [8]. This strategy is depicted in Fig.6 [4].

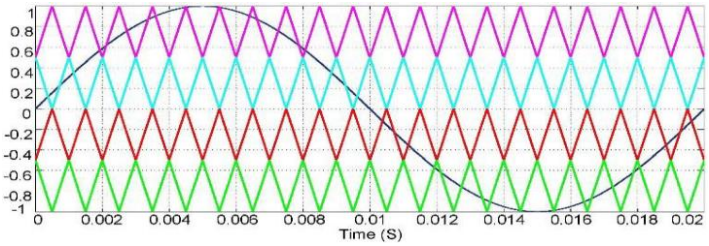


Fig.6. Alternate POD PWM

2.1.4 Phase Shift PWM (PS PWM)

This strategy is demonstrated, where all carrier signals have the same amplitude, frequency, and DC offset but are phase-shifted by 90 degrees as shown in below fig.7 [4].

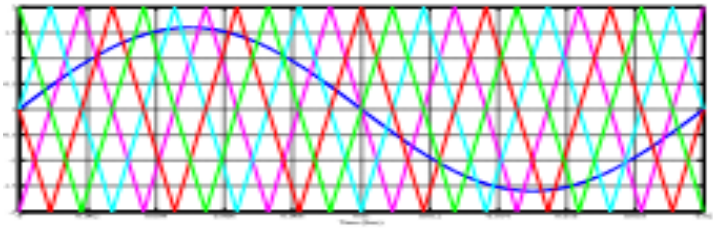


Fig.7. Phase shift PWM

2.1.5 Carrier overlapping PWM (CO PWM)

This approach for an N-level inverter uses N-1 carrier signals with the same frequency and peak to peak amplitude. The reference signal is placed in the centre of the carrier signals, and the carrier signals are organised so that the bands they occupy overlap each other and overlap until half of their amplitude is reached. This method is seen in fig.8 [9-10].

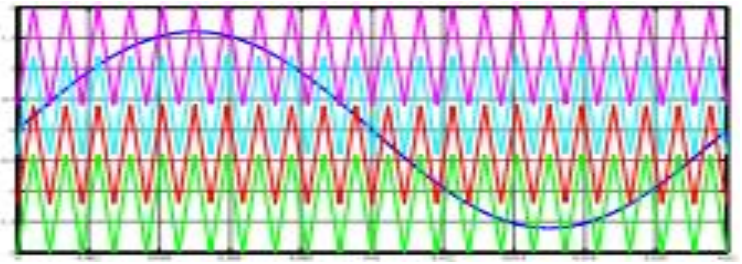


Fig.8. Carrier overlapping PWM

2.1.6 Multicarrier sinusoidal PWM with variable frequency

This approach is used to balance the number of switches in multilevel inverters where the switching frequencies of the top and bottom switches are greater than the switching frequencies of the intermediate switches. The carriers C1, C4 and C2, C3 have the same frequency in this case. [9-10].

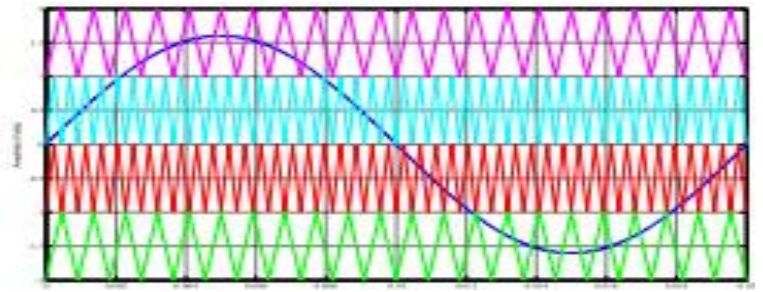


Fig.9. Multicarrier sinusoidal PWM with variable frequency

3 Simulink model

We employed the SPWM approach for a three-phase induction motor in this case. Figure 10 depicts the fundamental simulation diagram for the SPWM Phase disposition approach. For the CHBMLI of a seven-level inverter, it requires n-1 carriers, which are six carrier waves with the same frequency, amplitude, and phase, which are compared to a pure sinusoidal wave of fundamental frequency and pulses are formed. Figure 11 depicts the contrast.

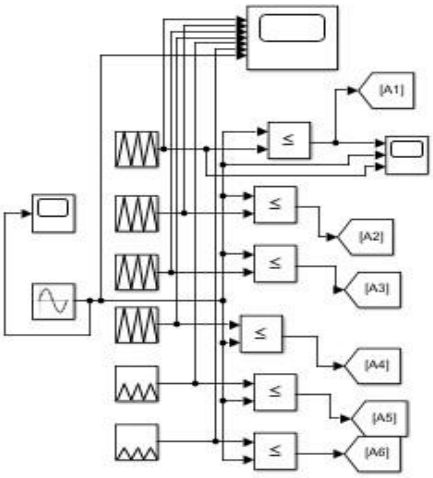


Fig.10. Matlab Simulink model of phase disposition of SPWM technique

These pulses are produced in order to power the three-phase induction motor. To create the switching pulses for three phase CHBMLI, three sinusoidal waveforms with a 120 degree phase shift must be compared with six sawtooth or triangular waves. As a result, each step of CHBMLI requires six pulses. The switching table for the CHBMLI is shown Table 1.

Table 1. Switching table of seven-level CHBMLI

Voltage level	Switches turn on
$3V_{dc}$	S_1S_2, S_5S_6, S_9S_{10}
$2V_{dc}$	S_1S_2, S_5S_6, $S_{10}S_{12}$ S_1S_2, S_6S_8, S_9S_{10} S_2S_4, S_5S_6, S_9S_{10}
V_{dc}	S_1S_2, S_6S_8, $S_{10}S_{12}$ S_2S_4, S_5S_6, $S_{10}S_{12}$ S_2S_4, S_6S_8, S_9S_{10} S_1S_2, S_5S_6, $S_{11}S_{12}$ S_1S_2, S_7S_8, S_9S_{10} S_3S_4, S_5S_6, S_9S_{10}
0V	S_1S_3, S_5S_7, S_9S_{11} S_2S_4, S_8S_6, $S_{10}S_{12}$
$-V_{dc}$	S_2S_4, S_6S_8, $S_{11}S_{12}$ S_2S_4, S_7S_8, $S_{10}S_{12}$ S_3S_4, S_6S_8, $S_{10}S_{12}$ S_3S_4, S_7S_8, S_9S_{10} S_3S_4, S_5S_6, $S_{11}S_{12}$ S_1S_2, S_7S_8, $S_{11}S_{12}$

$-2V_{dc}$	S_2S_4, S_7S_8, $S_{11}S_{12}$ S_3S_4, S_6S_8, $S_{11}S_{12}$ S_3S_4, S_7S_8, $S_{10}S_{12}$
$-3V_{dc}$	S_3S_4, S_7S_8, $S_{11}S_{12}$

By the sequence the switches will turn on and gives the output of seven level voltage as stepped waveform with the amplitudes of $3V_{dc}$, $2V_{dc}$, V_{dc},$-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$ as shown in fig.1.[8].

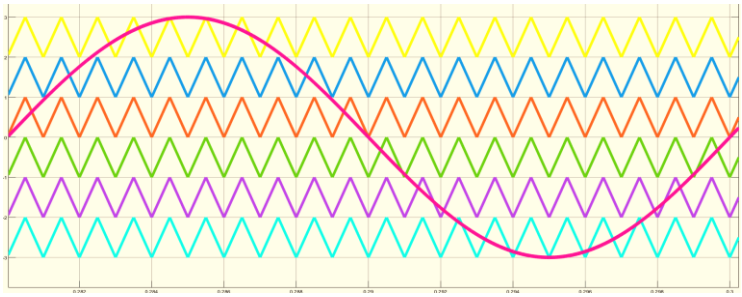


Fig. 11 Phase disposition SPWM

3.1 Specifications of circuit elements

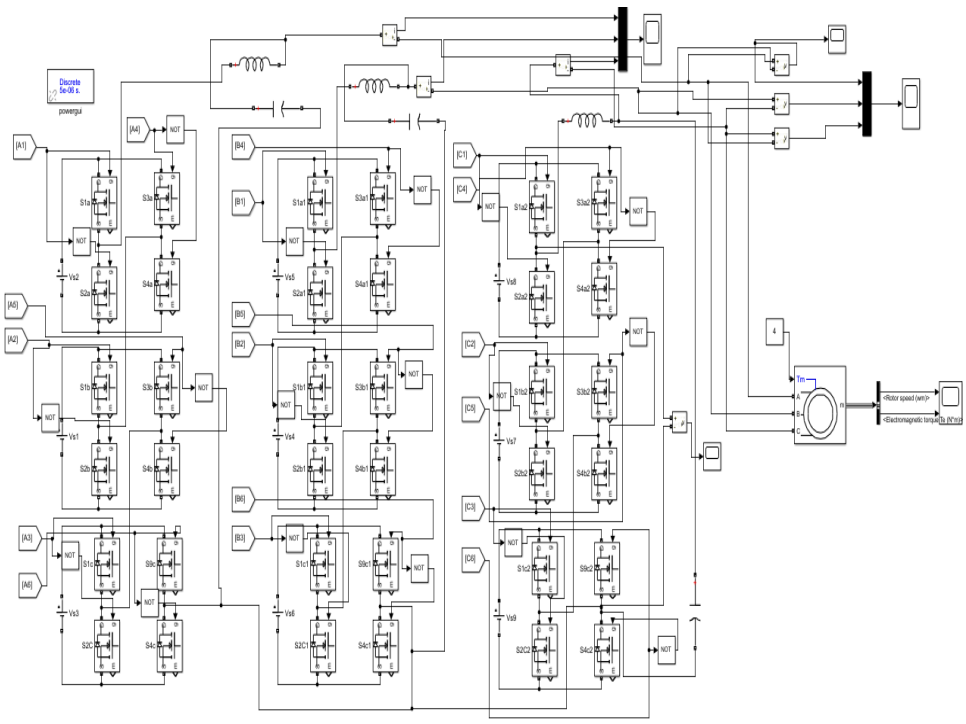


Fig 12 Simulation model of CHBMLI for three phase induction motor

The voltage provided to each H-Bridge by the input battery voltage source is 150 V, therefore each phase has three bridges supplied with 150 V. As demonstrated in fig. 13, the output voltage of CHBMLI is greater than 400V of phase voltage and the line

voltage of the three phase topology. The induction motor is rated at 3-ϕ, 400 V, 50 HZ, and 1500 rpm. L = 1H, C = 50nF are the design requirements for the LC filter. The switching frequency for the bridge's switches is 10KHZ.

3.2 Simulation results of generic method

Simulation process have been carried out for three phase CHBMLI with induction motor in open-loop control. The results of output voltage of three phase waveform, motor speed, torque, stator current, THD are shown below in fig 13-17.

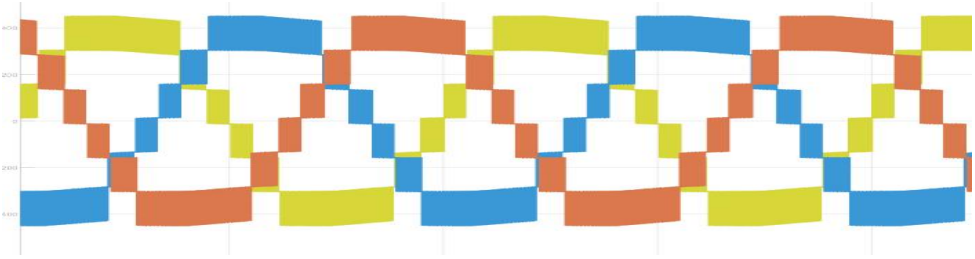


Fig. 13 Output phase voltage of seven level CHBMLI

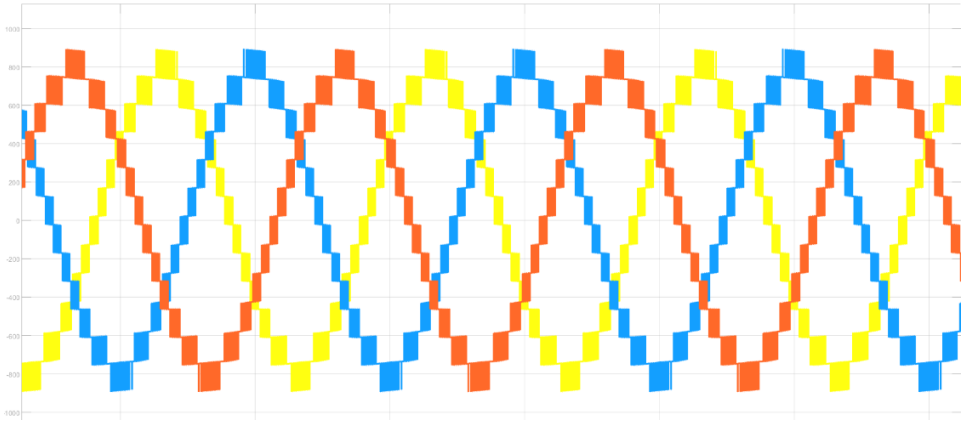


Fig. 14 Output line voltage of seven level CHBMLI

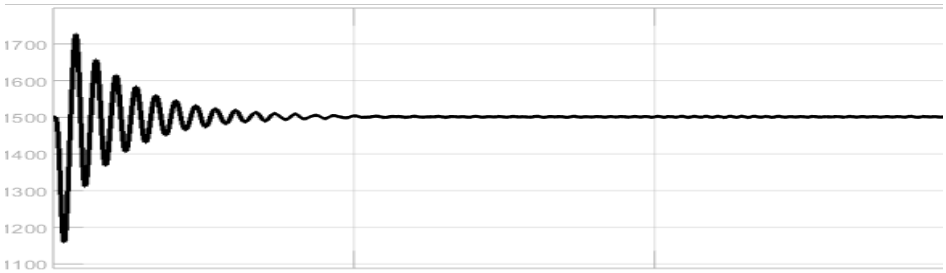


Fig.15 Speed of three phase induction motor

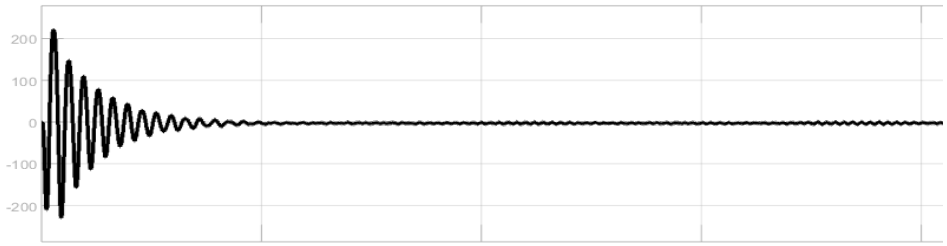


Fig.16 Electromagnetic torque of induction torque

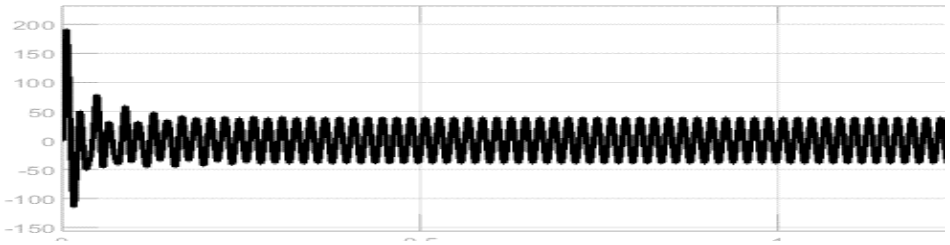
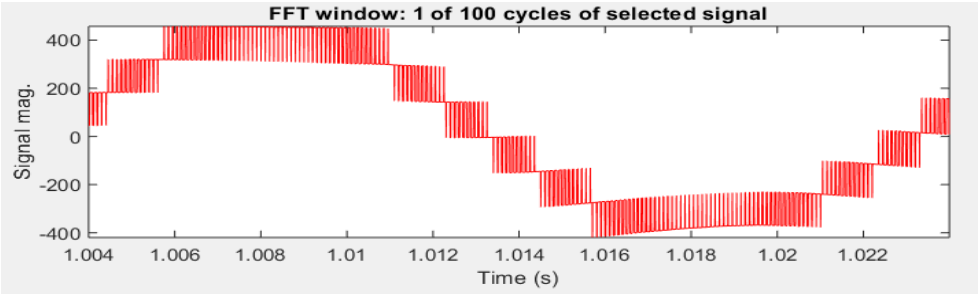


Fig.17 stator current of three phase induction motor



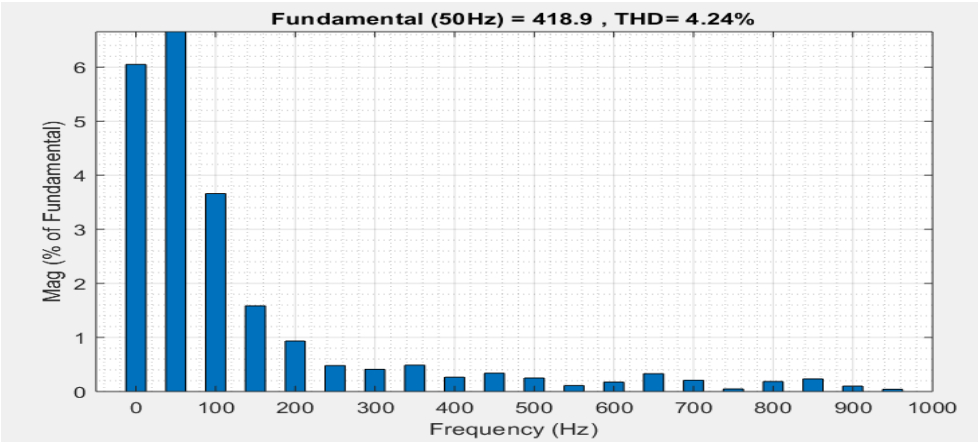


Fig.18 THD analysis

4 Conclusion

For the phase disposition method of sinusoidal pulse width modulation approach for an induction motor, the suggested seven level CHBMLI architecture has been designed. The fundamental advantage of using the PWM approach on an induction motor is that smooth performance is accomplished, and different outcomes such as output voltage, stator current, and so on are investigated. As the number of voltage levels is increased, the THD analysis of the output waveform improves; here, the THD is 4.2%.

References

1. Rao. J.S., Tummala S.K., Kuthuri, N.R., Nanotechnology for Environmental Engg., **7**, 393-403, (2022)
2. M. Leon.Tolbert, Fang Z. Peng, *Multilevel Converters for Large Electric Drives,* in preceedings of IEEE conference, (1998).
3. Rao S., Mn S.R., Syed S.N., Tummala S.K., *Gate driver circuit design, PWM signal genertaion using FEZ panda III and arduino for inverter*, E3S Web of Conferences, **87**, 01003, (2019)
4. R. Nagarajan, M. Saravanan, *Performance Analysis of Multicarrier PWM Strategies for Cascaded Multilevel Inverter*, in preceedings of European Journal of Scientific Research, December (2012).
5. Raju, N.A., Suresh Kumar T., Int. Jour. Of Innovative Tech. and Exploring Engg. **8**, 11, 3860-3864 (2019)
6. Satyanarayana, K., Gopal, A.V., Babu, P.B., Design optimisation of machining parameters for turning titanium alloys with taguchi-grey method, International Journal of Machining and Machinability of Materials, 2013, 13(2-3), pp. 191–202.
7. Satyanarayana Kosaraju, Swadesh Kumar Singh, Tanya Buddi, Anil Kalluri & Ahsan Ul Haq (2020) Evaluation and characterisation of ASS316L at sub-zero temperature, Advances in Materials and Processing Technologies, 6:2, 365-375
8. S. Krishnapriya, L. Unnikrishnan, Inter. Jou. of Resea. in Engg. and Tech., **04,** Sep (2015).
9. Suresh Kumar Tummala, Phaneendra Babu Bobba & Kosaraju Satyanarayana (2022) SEM & EDAX analysis of super capacitor, Advances in Materials and Processing Technologies, 8:sup4, 2398-2409,
10. Bidyut mahato, Rashmi kumari, Ravi raushan, Inter. Jou. of Res. in Engg and Tech, **04**, (2016).
11. Tummala, S.K., Indira Priyadarshini, T., Morphological Operations and Histogram Analysis of SEM Images using Python, Indian Journal of Engineering and Materials Sciences, 2022, 29(6), pp. 794–798.
12. Brendan Peter Mcgrath and Donald Grahame Holmes*,* IEEE Trans. on Indus Elect**., 49,** August (2002).
13. Suresh Kumar Tummala, Phaneendra Babu Bobba & Kosaraju Satyanarayana (2022) SEM & EDAX analysis of super capacitor, Advances in Materials and Processing Technologies, 8:sup4, 2398-2409
14. M.A.Saqib and S.A.R.Kashif, *"Artificial neural network Based Space vector PWM for a five-level diode-clamped inverter,"* AUPEC, (2010).
15. Davu, S.R., Tejavathu, R. & Tummala, S.K. EDAX analysis of poly crystalline solar cell with silicon nitride coating. Int J Interact Des Manuf (2022).