Design of Wallace tree multiplier circuit using high performance and low power full adder

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Abstract: The act of multiplying includes adding partial products repeatedly, and conventional multipliers call for many adders to perform partial product addition in higher order multiplication. A multiplier's effectiveness and efficiency are evaluated using parameters such as speed, time delay, area, Power Delay Product (PDP), accuracy, and power consumption. In order to choose the optimum multiplier, this project is to evaluate various multipliers their performance metrics. Then, suggests employing a hybrid technology-based adder to improve the performance of the selected multiplier. The power consumption of the multiplier can be significantly reduced while maintaining the required accuracy by using a hybrid technology-based adder and low power full adders. This will allow multipliers to be used in low-power applications where power consumption is a major concern. To summarize, the goal of this project is to design and compare different multipliers using H-spice coding, as well as to improve the performance of the chosen. This project used 4x4 multiplier evaluation using 32nm technology.

1 INTRODUCTION

The world keeps changing and new technology is evolving every ticking second. As the world keeps changing and advancing, many advancements are also made in digital signal processing and artificial intelligence. These are some of the key aspects of development. We can see that signal processing and AI are moving to next level by new inventions being made. Here, the role of multiplier comes into action. Multiplier is a key element in any DSP application [1].

Multiplier plays a major role in Digital Signal Processing and Embedded systems applications. In Digital Signal Processing [2], multiplier is a main part of processor. Processor is like brain of the system. It is the unit responsible for processing all the instructions and responding accordingly. multiplier is a device used to amplify different signals as per requirement.

Along with its role in processor, multiplier is also one of the biggest power consumers in any processer it is present in. Multiplier is used to build energy efficient devices and

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compact devices. That depends on the type of multiplier used for a particular application. There are different types of multipliers for different application. A particular multiplier is taken based on its features and observing its compatibility with the processor. Multipliers are used in various applications. Some of them are arithmetic operations in ALU, Modulation and demodulation of signals,Voltage divider Amplification of signal and Image processing.

The performance of multiplier decides the performance of processor. Multipliers are one of major sources of power dissipation. But they have a crucial role to play in processors. Hence, we need to find a way to reduce the power dissipation and increase the efficiency of the system so that the processor can meet the needs of power utilization. Multiplier performance is directly linked to the performance of the adders used in it [3]. So, we can decrease the power dissipation and increase the efficiency of processor by concentrating on the internal adders and circuit of multiplier.

The basic structure of a multiplier is easily understandable and consists of mainly adders and and-gates considering its logic diagram. These are the basic structures of multiplier. Any changes cannot be made to an and-gate which itself is the most basic structure. So, here in this project; Adders which are made up of xor and xnor gates are concentrated on, which can be modified [4].

This project includes analysis of the designed multiplier and seeing that it is applicable to many tasks. This project mainly focuses on power consumption, delay, and size of multiplier for comparison and deciding the best multiplier out of basic multipliers we generally use. Low power and high-speed multipliers are necessary for high-speed DSP applications [5]. Since considering power and delay gives different outputs for best multiplier, this project considers the product of those two as a metric for our comparison. This gives the best multiplier which can be applicable for many purposes. Then the performance of the best multiplier is tested using a new hybrid adder [6].

The result of this project is to check if the performance of our desired multiplier can be further improved by using new technology and approaches to make it a better multiplier compatible to new age applications [7].

1.1 LITERATURE SURVEY

Multiplication, a crucial function in digital circuits, necessitates continuously adding imperfect products. Conventional multipliers use several adders to do partial product addition in higher order multiplication, which leads to excessive power consumption. A multiplier's effectiveness and efficiency are measured using a number of performance metrics, including speed, time delay, area, Power Delay Product (PDP), accuracy, and power consumption. Additionally, it suggests utilising a hybrid technology-based adder to improve the performance of the selected multiplier.

Multiple studies have evaluated different multipliers using Hspice coding and other performance metrics. For instance, Yu et al.'s (2019) study evaluated the performance of various multipliers, including the array, Wallace, and Booth multipliers. The investigation showed that the Booth multiplier operated at the fastest speed, while the Wallace multiplier consumed the least amount of electricity. Similar to this, Huang et al.'s study from 2019 used a range of complete adder designs to evaluate the effectiveness of different multipliers. The study found that the adoption of low power full adders significantly reduced the power

consumption of the multiplier. Several studies have recommended employing a hybrid technology-based adder to improve the effectiveness of the selected multiplier.

2 OPERATION OF THE SYSTEM

This project deals with the operation of multipliers. Different multipliers have different approaches to find the required output. The functionality of multiplier is better understood when the logic used in it is understood.

2.1 ARRAY MULTIPLIER

The array multiplier's logic as shown in fig.1 is essentially the same as the normal multiplication process we use. Three main steps make up an array multiplier's multiplication process: partial product production, partial product reduction, and final addition. The multiplicand is added to an accumulator and the multiplier bit is shifted to the right while the multiplicand bit is changed to the left when the multiplier's least significant bit (LSB) is set to 1. Up until all of the multiplier bits are zero, this operation is repeated.

Partial products can be added serially to save hardware, but a parallel multiplier can add all partial products. However, using a compression technique, the number of partial products can be reduced before addition. The "add and shift" algorithm is the most commonly used multiplication method. AND gates are used to generate the partial products, with the multiplicand being N-bits, the multiplier being M-bits, and the partial products being N*M.

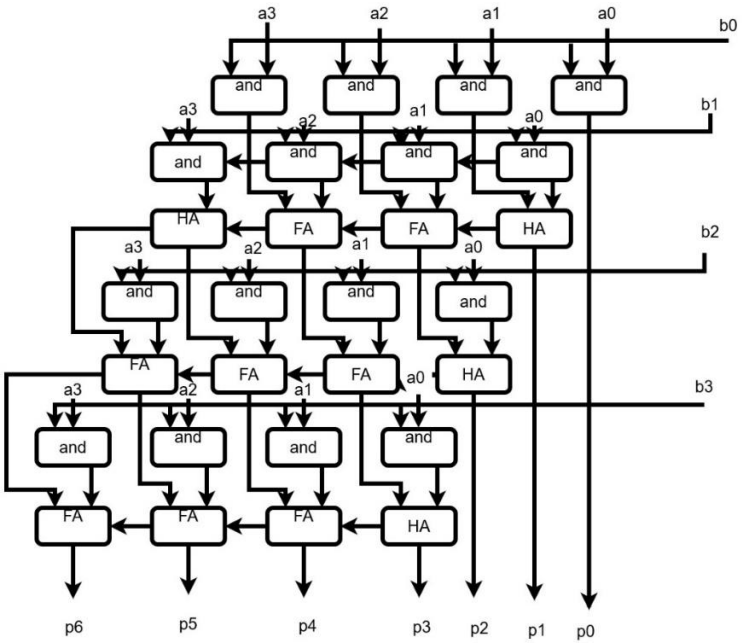

Fig. 1. Array multiplier circuit.

The process which is executed is explained using mathematical representation below. Take multiplier and multiplicand as a3a2a1a0 and b3b2b1b0, respectively

Multiplication:

```
                b3  b2   b1   b0
                a3   a2    a1   a0        X
              ---------------------------------------

                        a0b3  a0b2  a0b1  a0b0
                   a1b3  a1b2  a1b1  a1b0
              a2b3  a2b2  a2b1  a2b0
         a3b3  a3b2  a3b1  a3b0
```

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c7 c6 c5 c4 c3 c2 c1 c0

In similar way array multiplier also calculates partial products and add them to give us required output.

2.2 WALLACE TREE MULTIPLIER

The Wallace tree multiplier as shown in fig.2 is a multiplication algorithm with three major steps. In the first step, an AND gate is used to multiply each bit of one number by each bit of the other number. This yields a collection of partial products. These partial products are reduced to two numbers in the second step. This is accomplished by layering wires of similar weight together. If three or more wires of the same weight are present, they are fed into a Full Adder. If only two wires of the same weight are present, they are fed into a Half Adder. Finally, if only one wire remains, it connects to the next layer.The two resulting numbers from the second step are fed into an adder, which computes the final product, in the third and final step [8].

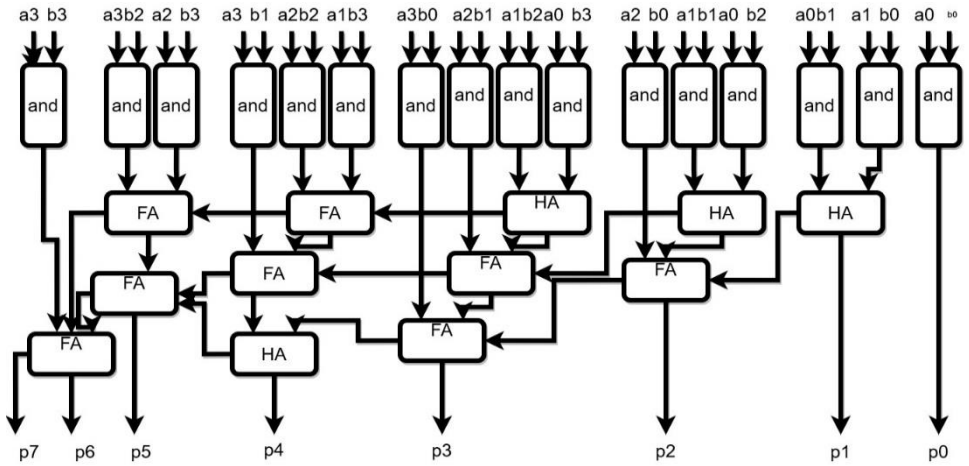

Fig. 2. Wallace Tree multiplier circuit.

Unlike other multiplication algorithms, the Wallace tree multiplier generates all partial products first and then adds them in steps. This method reduces the number of adders required to perform the multiplication, resulting in a more efficient algorithm. In this multiplier, taking a multiplier and a multiplicand as a3 a2 a1 a0, b3 b2 b1 b0 the multiplication process is presented below.

Multiplication:

```
                b3  b2   b1   b0
                a3   a2    a1   a0        X
              ---------------------------------------
                        a0b3  a0b2  a0b1  a0b0
                   a1b3  a1b2  a1b1  a1b0
              a2b3  a2b2  a2b1  a2b0
        a3b3  a3b2  a3b1  a3b0                                          Level-1
```

```
              c5     c4     c3     c2     c1     c0
        a3b3  a3b2  a3b1  a3b0
Level-2
```

```
p7     p6     p5     p4     p3     p2     p1     p0      Final Output
```

It has same no. of multiplications and additions as array multiplier but the logic is different. The logic makes it consume less power and hence makes it better than the array multiplier

2.3 Bough Wooley Multiplier

In Bough Wooley Multiplier as shown in fig.3, instead of performing a subtraction operation, another method for calculating the final product is to compute the 2's complement of the last two terms and add all of them together. The final two terms are n-1 bits long and range in binary weight from position 2 to 2^(n-1).

The final product, on the other hand, is 2n bits long and ranges in binary weight from 2^0 up to 2^(2n-1). The final product can be obtained using a single addition operation by adding all the terms together after computing the 2's complement of the last two terms. This approach may be preferred in some applications because it simplifies the overall computation and reduces the number of operations required.

3 PROPOSED WALLACE TREE MULTIPLIER

The above mentioned three multipliers work well according to the application. But, when compared their power and delay, it is proven that Wallace tree multiplier works best out of all three. So, it is taken for this project. The power delay product of Wallace tree multiplier can be further improved using the hybrid full adder circuit[1] as shown in fig.4. In this study XNOR and XOR circuits were proposed. In XNOR and XOR circuits, level-restoring transistors P4 and N4 are used to give full swing output for all possible input configurations

[9]. These circuits run faster and use less power because the crucial path doesn't have any NOT gates. These circuit have the ability to drive as well.

A mixture of the XOR and XNOR circuits, the suggested circuit for simultaneous XOR-XNOR produces a low-power, quick circuit with good driving capability and full swing output. Only 12 transistors are used in this circuit, and there are no NOT gates on the crucial route, making it very energy-efficient.

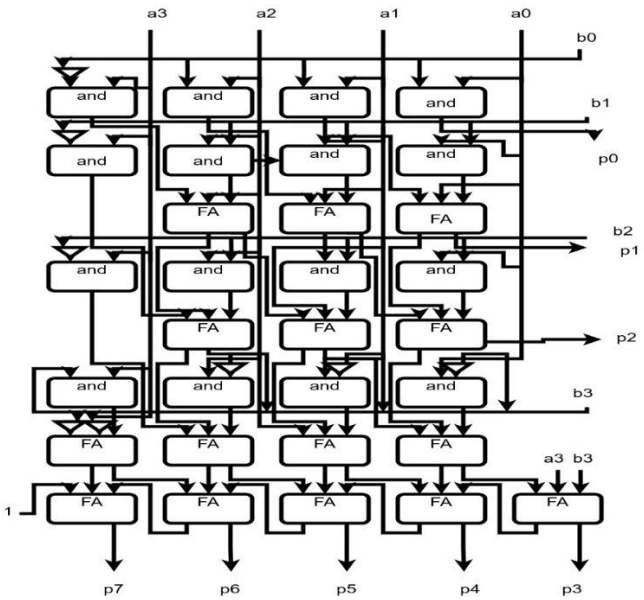

Fig. 3. Bough Wooley multiplier circuit

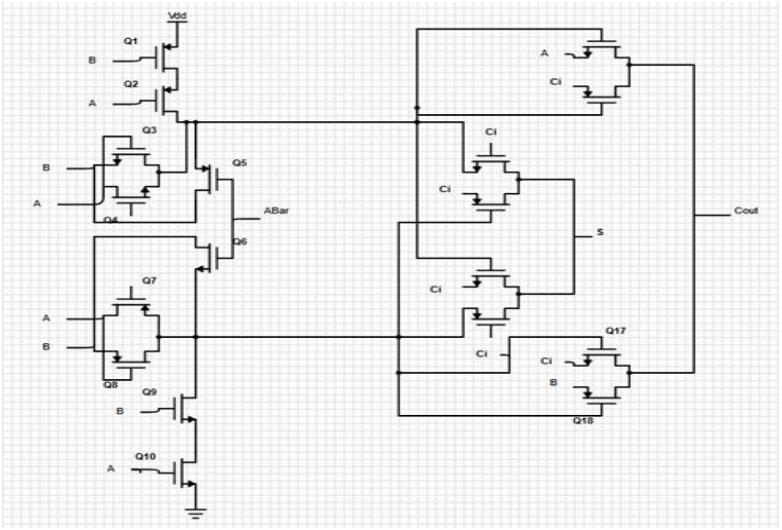

Fig. 4. Hybrid Full Adder.

Using the suggested circuit, the authors developed six novel hybrid full adders that employ hybrid logic. Each of these full adders uses a 2-to-1 multiplexer structure as well as the proposed XOR, XNOR, or simultaneous XOR-XNOR circuit [10]. The 2-to-1 MUX arrangement reduces static and short circuit power consumption by utilising transmission gates and only four transistors.

The first proposed full adder, HFA20T, employs a simultaneous XOR-XNOR circuit and two 2-to-1 MUX structures, resulting in a 20-transistor circuit. The absence of high-power-consuming NOT gates in the critical path results in high speed and low power dissipation [11]. This full adder has a full swing output and can withstand supply voltage scaling. While this circuit's driving capability decreases when used in cascaded structures, it remains the best of all the proposed full adders in the paper and is used in this project.

4 RESULTS AND DISCUSSIONS

Initially Firstly, the three chosen multipliers namely Array multiplier, Baugh Wooley multiplier, and Wallace tree multiplier are compared using the conventional adders and the conventional circuit using Hspice simulation tool. The simulation is done to compare power consumption, and delay of those three multipliers and choose the best multiplier out of those three using power-delay product as metric [6]. The comparisons are as following.

Table 1. Comparison of three multipliers using conventional adder.

NAME OF THE MULTIPLIER	DELAY (NANO SEC)	POWER CONSUMPTION (MICRO WATTS)	NO OF ELEMENTS	PDP
Array Multiplier	4.1856	24.388	601	102.0857
Wallace Tree Multiplier	5.0970	17.483	601	89.1108
Bough Wooley Multiplier	3.3765	29.919	895	101.0215

From the Table 1, we can observe that wallace tree multiplier has better power delay product. Hence, it is chosen to be the best multiplier out of the three multipliers under test.The best multiplier, which is wallace tree multiplier is then redesigned using hybrid full adder. For better understanding, all the multipliers are redesigned using the hybrid full adder and the results are presented in table2.

From the table 2., it is clearly stated that the wallace tree multiplier is best even with the new hybrid full adder and it is infact a lot better than the conventional wallace tree multiplier. To observe the comparisons in a better way, let us observe the power, delay and power delay product comparison graphs.

Table 2. Comparison of multipliers using hybrid full adder.

NAME OF THE MULTIPLIER	DELAY (x10^-9)Sec	POWER CONSUMPTION (x10^-5) Watts	PDP (x10^-15) Watt-Sec
Conventional Wallace Tree Multiplier	5.0970	1.7483	89.1108
Array Multiplier using Hybrid Full Adder	2.4632	1.1195	27.575
Wallace Tree Multiplier using Hybrid Full Adder	0.10662	1.3694	1.4600
Bough Wooley Multiplier using Hybrid Full Adder	4.1866	1.0410	43.5825

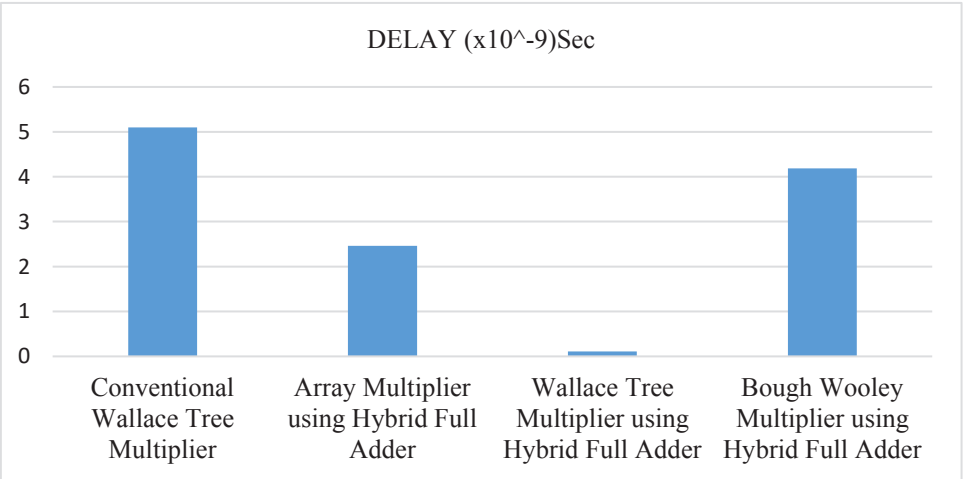

Fig. 5. Delay comparison of mutipliers.

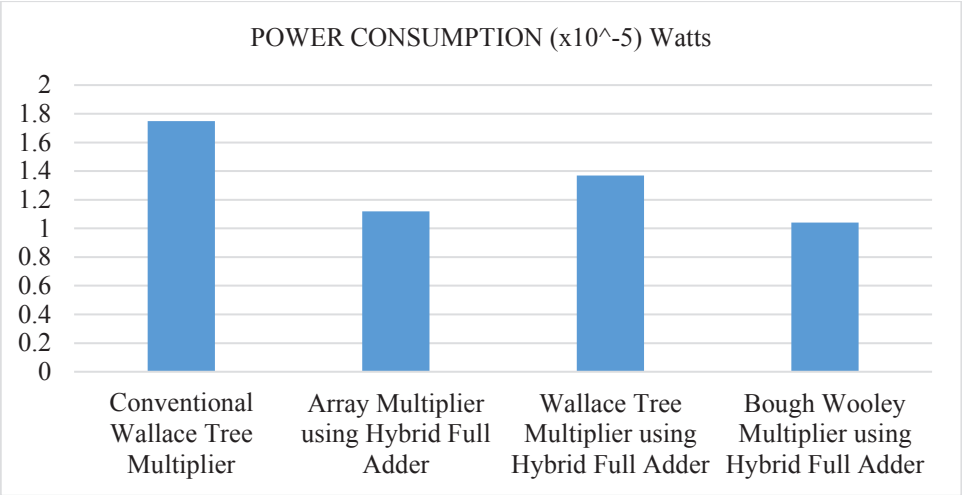

Fig. 6. Power consumption comparison of multipliers.

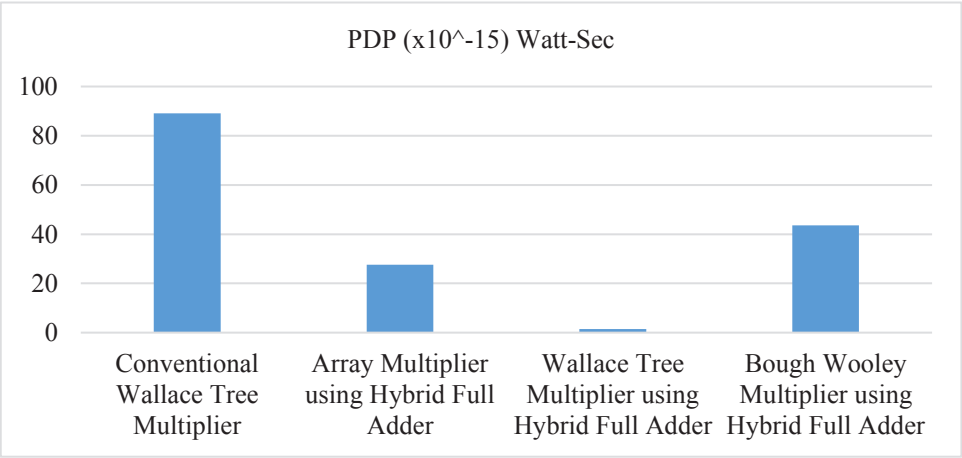

Fig. 7. Power delay product comparison of multipliers.

Comparison of power,delay and PDP are shown in fig.5, fig.6, fig.7 respectively.This above comparison graphs gives us the better understanding of the project and the outcomes.

5 CONCLUSION

After a thorough analysis of various multipliers in terms of power consumption, delay, and PDP. it was found that the Wallace tree multiplier using a hybrid full adder exhibited the lowest power consumption and delay. However, the selection of an appropriate multiplier for a particular application must be made based on the application constraints. Further experimentation was conducted with all multipliers utilizing a hybrid full adder, which led to the discovery that higher technology full adders yielded better results. This finding may serve as a useful guideline for future multiplier designs. It is noteworthy that the logic of the Wallace tree multiplier outperformed the remaining multiplier circuits even when other adder

circuits were used. This finding highlights the potential benefits of utilizing the Wallace tree multiplier for various applications.

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