Improving the Stability of Cascaded DC Power Supply System by Adaptive Active Capacitor Converter

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Abstract - When all links are changes in the cascade is the corner of the shape in the dc division energy orbit (DEO). When resistances are intermission betwixt one by one stylish changes in that would possibly end up so the cascaded orbits are unsteady. They are antecedent we can place in a nearer to the useful in the cascaded orbit can be got in compelled to vary the supply they have load changes in the internal structure of the same regions in the electrical device they can be opposed in a quality of the characteristic of dc DEO. Throughout the Associate in nursing adaptation active device in the (AACC) we can know another determined in the cascaded orbit. Therefore the AACC was connected by side by side in the cascaded orbit's they can mediate in between the carries and completely a requirement of a notice then they carries the voltage with none modification in this subsystems. when the cascaded orbits have their quantity of it slowly it will extend in time. They have activity fundamental truth to stop their magnificence thought in the AACC are mentioned throughout of this project, it can have four thousand eight hundred and zero watts cascaded orbit was contain a strive of process to move in a full-bridge changes they can be styli shed and evaluated. So when the simulation solutions have to clear the performance of the arrangement of AACC.

Index Terms—Active capacitor converter, adaptive control, cascaded System, modularization, stability.

1. Introduction

The dc division energy orbit (DEO) has been used widely in such applications as space stations, aircraft, communication systems, industrial autonomous production lines and

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defense electronic power systems for the last 20 years [1]–[5], due to its flexile system configuration, high-efficiency energy conversion, and high-density power delivery capability .One of the dc DEO'S attractive characteristics is modularity design[6], in which each Subsystem is first designed individually as a module, and then all subsystems are integrated to form a dc DEO. The modularization characteristic of dc DEO cuts down the system's development cycles and costs effectively. In a dc DPS, there are various ways to connect the subsystems, among which, a typical connection style is cascaded converts.

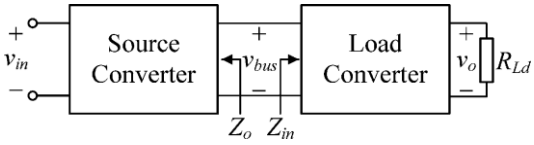

Fig. 1. Cascaded power supply system.

The cascaded system may have stability problem due to the interaction between the subsystems, even though each subsystem is individually well designed to be stable on its own [7]–[10]. was shown that for the typical cascaded system shown in Fig. 1, the ratio of the source converter's output impedance *Zo* and the load converter's input impedance *Z*in*, Zo* /*Z*in , can be equivalently represented as the loop gain of the cascaded system. It was also pointed out that if both the ource converter and the load converter are stable individually, and *Zo* is less than *Z*in in the entire frequency ranges, the stability of the cascaded system will be guaranteed. This is the so-called Middle brook criterion. Subsequently, various impedance criteria aiming at a more accurate and practical prediction of the subsystem interaction had been developed in the last two This paper first analyzes the impedance characteristics and instability problem of the cascaded system in Section II, and presents the concept, operating principle, ad control strategy of AACC in Section III. The design procedure and a design ample of AACC are given in Section IV. Section V shows he experimental results that verify the effectiveness of the proposed method.

2. Impedance Characteristics and Instability Problem of Cascaded System

A. Review of Subsystem's Impedance Characteristic And Cause of Instability

For cascaded systems, the impedance characteristics of subsystems and the cause of instability have been studied extensively during the last two decades. Some general conclusions are summarized as follows:

1) Impedance characteristic of *Zo* : *Zo* is the source converter's output impedance independent of its load resistor. As shown in the dotted line of Fig. 2, *Zo* is similar to the output impedance of an *LC* filter. If*f* < *fc S, Zo* presents the characteristic of an inductor; and if *f* > *fc S, Zo* presents the characteristic of source converter's output filter capacitor. Here, *fc S* is the cutoff frequency of the source converter's voltage loop. Note that *Zo* 's peak value ,*Zo* peak, appears at *fc S* and is inversely proportional to source converter's output filter capacitor.

2) Impedance characteristic of *Z*in : In Fig. 2, the solid line Represents *Z*in that is the input impedance of load converter Operating in continuous current mode (CCM). If*f* < *fc L, Z*in behaves as a negative resistor, whose value equals to $-V$ 2 bus*/Po* , where *V*bus is the intermediate bus voltage and *Po* is the load converter's output power

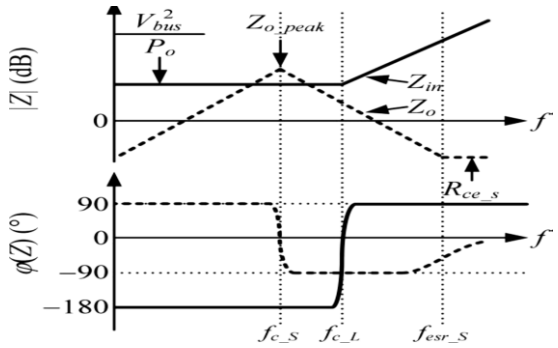

Fig. 2. Impedance interaction of the cascaded system

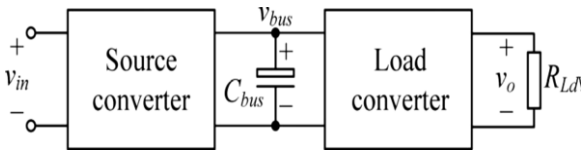

Fig. 3. Cascaded system with additional intermediate bus capacitor

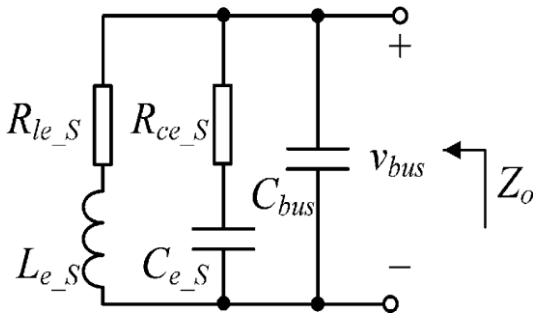

Fig. 4. Equivalent model of *Zo* with additional intermediate bus capacitor

and if $f > fc\ L$, *Z*in behaves as an inductor. Here, *fc L*is the cutoff frequency of the load converter's voltage loop. Note that when $f < fc\ L$, the magnitude of *Z*in is inversely proportional to *Po* [32].

B. Solving the Instability Problem by Adding Intermediate Bus Capacitor

There is nothing more desirable than a total separation between *Zo* and *Z*in to ensure that the cascaded system is stable. Since |*Zo* peak| is inversely proportional to source converter's output filter capacitor [30], one intuitive way is to reduce the source converter' output impedance by adding an intermediate bus capacitor *C*bus to the cascaded system, as shown in Fig. 3.Here, *C*bus can be treated as an additional output filter capacitor of the source converter, and the equivalent *LC* output impedance model of source converter with *C*bus is given in Fig. 4. In Fig. 4, *Le S* is the equivalent filter's inductor, *Ce S* is the equivalent filter's capacitor, *Rle S* is the parasitic resistor of

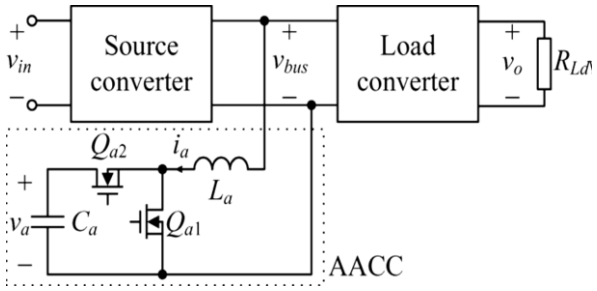

Fig. 5. Topology of the AACC introduced into cascaded system

Le S , and *Rce S* is the equivalent series resistor (ESR) of *Ce S* that can be measured from Fig. 2. Also, *Ce S, Le S* , and *Rle S*
are expressed in (1)–(3), respectively

$$Ce\ S = 1/2\pi Rce\ S\ f\text{esr}\ S \quad (1)$$

$$Le\ S = 1/(2\pi fc\ S)2\ Ce\ S \quad (2)$$

$$Rle\ S = Le\ S/Ce\ S \cdot |Zo\ \text{peak}| - Rce\ S \quad (3)$$

where *f*esr *S* is the zero caused by the ESR of *Ce S* . According to (1)–(3), the peak value of *Zo* in Fig. 4 is derived as

$$|Zo\ \text{peak}| = Le\ S/(Ce\ S + C\text{bus})\ (Rle\ S + Rce\ S)\ . \quad (4)$$

Thus, in order to ensure that $Zo < Z$in the entire frequency ranges, |*Zo* peak| must satisfy

$$|Zo\ \text{peak}| \le V\ 2\text{bus}/Po \quad . (5)$$

From (4) and (5), the required value of *C*bus can be obtained as

$$C\text{bus} \ge Le\ SPo/V\ 2\text{bus}\ (Rle\ S + Rce\ S) - Ce\ S. \quad (6)$$

According to (6), the required *C*bus increases with the increase of *Po* , so, if a capacitor is employed, its value must be selected by (6) at full load. However, a larger *C*bus results in a smaller bandwidth of the source converter that is already modularly designed, In this way, the cascaded system does not only ensure stable, but also achieves a better dynamic response.

3. TOPOLOGY AND CONTROL OF THE PROPOSED AACC

A. Topology of AACC

The adaptively varying *C*bus mentioned in Section II can be Emulated by a converter, as shown in the dashed block in Fig. 5.The converter is referred to as AACC. The AACC is composed of switches *Qa*1 and *Qa*2 , inductor *La* , and capacitor *Ca*. It is connected to the intermediate bus of the cascaded system. By controlling *La* 's current appropriately, the terminal characteristic at the bus side of AACC will present an adaptively varying *C*bus that ensures the stability of the cascaded system and improves the dynamic response.

The AACC is also suitable for the cascaded system with multiple load converters. In this case, the AACC has the same operation principle with the system of Fig. 5, which just makes the source converter's output impedance lower than the total input impedance of the multiple load converters.This paper analyzes the case shown in Fig. 5, but the conclusion applies to the system with multiple load converters.

B. Control of AACC

Since the function of AACC is to emulate the adaptive *C*bus, the current of *La, ia* , should be controlled as

$$ia\ (t) = C\text{bus}(dv\text{bus}/dt) \quad . (7)$$

According to (6) and (7), it can be known that *ia* varies with *Po* . Considering *Po* can be reflected by the oscillation ripple of *v*bus, Δ*v*bus [13], *ia* could be controlled by Δ*v*bus, whose control cicuit is realized by a simple analog circuit, as shown in Fig. 6. The control circuit for *ia* would only need to detect *v*bus without changing any part of the existing subsystems. Thus, the AACC can be designed as a standard module for dc DPS.As shown in Fig. 6, *v*bus first goes through a differential circuit (sub circuit A) to get the form of *ia* ref (*dv*bus/*dt*), defined as *v*1 . Meanwhile, Δ*v*bus is extracted from *v*bus by the filter comprising *C*2 and *R*5 , and then it is sent to the rectifier circuit. The shutdown signal of UC3525 is generated by sub circuit F that determines the working mode of AACC automatically. If the

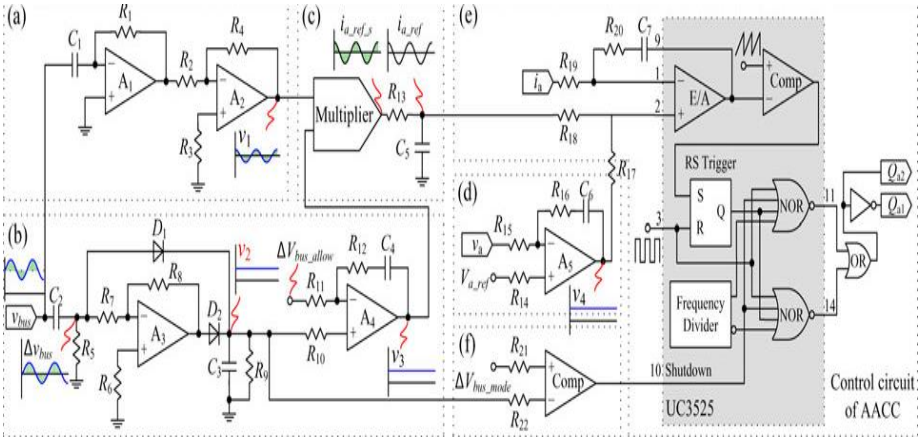

Fig. 6. Control circuit of the AACC

Cascaded system is unstable, the magnitude of Δ*v*bus*, v*2 , will be larger than the permitted value, denoted as Δ*V*bus mode, and the shutdown signal of UC3525 will become low. In this case, the AACC works normally. Otherwise, the shutdowns signal will go high, shutting down the AACC. Here, Δ*V*bus mode is set at a value below Δ*V*bus allow to ensure that AACC works well.

4. DESIGN OF AACC

A. Output Filter Capacitor Ca

With AACC, ignoring the switching harmonics of the cascaded system's intermediate bus voltage, *v*bus can expressed as

$$v\text{bus} = V\text{bus} + \Delta V\text{bus allow} \sin \omega t. \quad (8)$$

Where *V*bus is the average value of *v*bus, and ω is the angular
Frequency of the ripple in *v*bus, i.e., $\omega = 2\pi fc$ *S* .
The instantaneous input power of AACC can be obtained by (7) And (8), i.e.,

$$pa(t) = v\text{bus}ia$$
$$= (V\text{bus} + \Delta V\text{bus allow} \sin \omega t)C\text{bus}\Delta V\text{bus allow}\omega \cos \omega t. \quad (9)$$

Generally, Δ*V*bus allow _ *V*bus; thus, (9) can be simplified as

$$pa(t) = V\text{bus}C\text{bus}\Delta V\text{bus allow}\omega \cos \omega t. \quad (10)$$

According to (7) and (10), the waveforms of the instantaneous input power *Pa* ,inductor current *ia* , and output filter capacitor voltage *va* of AACC are depicted in Fig. 7. It can be seen that *Ca* is discharged from *Tos* /4 to 3*Tos* /4, and *va* decreases; and *Ca* is charged from

3*Tos* /4 to 5*Tos* /4, and *va* increases. Consequently, the maximum and minimum values of *va* occur, respectively, at*Tos* /4 and 3 *Tos* /4.
The energy charging *Ca* from 3*Tos* /4 to 5*Tos* /4

$$\Delta E_a(t) = \int_{\frac{3Tos}{1}}^{t} P_a\,(t)dt$$

$$= \int_{3Tos/1}^{t} V_{bus}\, C_{bus} \Delta V_{bus\_allow} \omega\, cos\, \omega t\, dt$$

$$= 2V_{bus} C_{bus} \Delta V_{bus\_allow} sin^2\left(\frac{\omega}{2t} + \pi/4\right) \qquad (11)$$

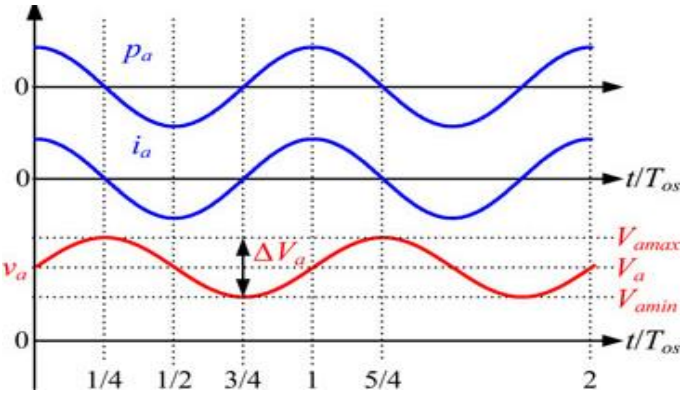

Fig. 7. Waveforms of instantaneous input power, inductor current, and output filter capacitor voltage of the AACC.

Here, Δ*Ea* (*t*) can also be expressed as

[ΔEa (t)=1/2CaV]_a^2(t) -1/2CaV]_(a min) ^2

where *Va* min is the minimum voltage of the capacitor *Ca* . Putting (12) in (11) gives

[1/2Ca [V〗 _a^2(t) - V_ (a min) ^2] =2 VbusCbus ΔVbus_allow Sin2 (ω/2t +π/4) (13)

From (13), we have

$$V_a(t) = \sqrt{\frac{4VbusCbus\Delta Vbus_{allow} Sin2\left(\frac{\omega}{2t}+\frac{\pi}{4}\right)}{Ca} + V_{a\,min}^2} \qquad (14)$$

Substitution of *t* = 5*Tos* /4 into (14), the maximum voltage of the capacitor *Ca* can be derived as

$$V_{a\,max} = \sqrt{\frac{4V_{bus}C_{bus\Delta V_{bus\_allow}}}{C_a} + V_{a\,min}^2} \qquad (15)$$

The average voltage of *Ca* can be approximated as

Vabc = (Va min + Va max)/2

$$= V_{a\,min} + \frac{\sqrt{4\,V_{bus}\,C_{bus}\Delta V_{\frac{bus_{allow}}{C_a}} + V_{amin}^2}}{2} \qquad (16)$$

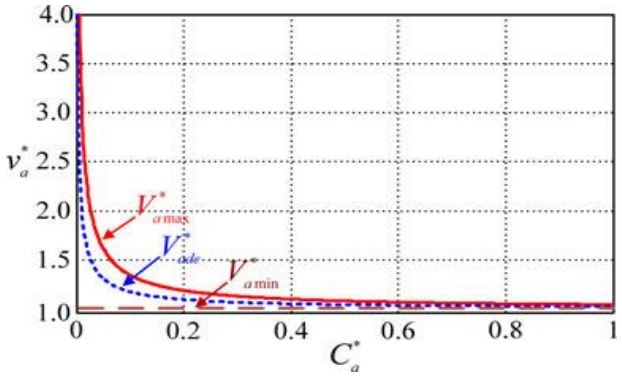

Fig. 8. Plots of $V*a$ max, $V*a$ min, and $V*a$dc as functions of $C*a$.

To ensure the proper operation of AACC, the instantaneous Voltage of *Ca* must always be higher than the input voltage of AACC, i.e.,

$$va\,(t) \geq V\text{bus}. \tag{17}$$

We set *Va* min at *V*bus and Δ*v*bus allow at 1% × *V*bus, and the Normalized *Va* max and *Va* dc with base of *V*bus are

$$V\_(a\ max)\text{^}*=V\_(a\ max)/V\_bus=\sqrt{(4\%/C\_a\text{^}*)}+1 \tag{18}$$

$$V\_abc\text{^}*=V\_abc/V\_bus\ =1/2+\sqrt{(4\%/C\_a\text{^}*\ )}+1/4 \tag{19}$$

Where $C*a$ is the normalized *Ca* with base of *C*bus. According to (18) and (19), $V*a$ max and $V*a$dc as functions of $C*a$ are plotted in Fig. 8. Here, *Va* max increases as *Ca* reduces. In order to adopt film capacitors or ceramic capacitors instead of electrolytic capacitors, the value of *Ca* should be small enough However, this will result in high *Va* max. A high *Va* max induces high voltage stress on *Qa*1 and *Qa*2 . Thus, *Ca* needs to be selected eclectically. Note that *Ca* must be selected at full load because it is the worst case for the cascaded system and the required *Ca* has the maximum value.

B. Selection of Qa1 and Qa2

According to Fig. 5, the voltage stress of *Qa*1 and *Qa*2 is the Maximum voltage of *va* , i.e.,

$$VQa\ 1 = VQa\ 2 = Va\ \max. \tag{20}$$

The current stress of *Qa*1 and *Qa*2 is the maximum current of *La* , and can be derived from (7) and (8), i.e.,

$$IQa\ 1 = IQa\ 2 = \omega C\text{bus max}\Delta V\text{bus allow} \tag{21}$$

Where *C*bus max is the required value of *C*bus at full load. The power devices for *Qa*1 and *Qa*2 could be chosen according to (20) and (21).

C. Inductor of AACC

Two factors must be taken into consideration when choosing the value of *La* . One is to ensure that the inductor current is

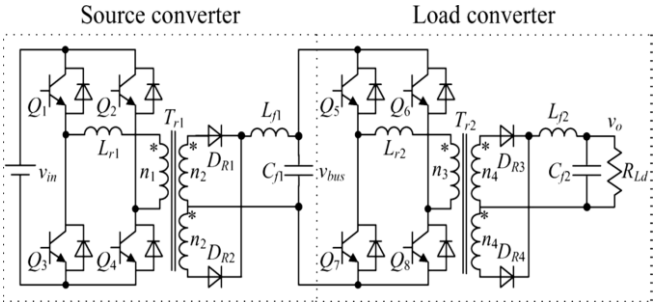

Fig. 9. Cascaded system consisting of two phase-shifted full-bridge converters.

Capable of tracking the current reference and the other is that the inductor current ripple should be kept small. Here, the AACC's inductor current, *ia* , needs to track the
Oscillation ripple, whose oscillation frequency is the cutoff frequency of the source converter's voltage loop gain. Hence, the switching frequency of AACC, *fsa* , should be chosen much higher than the oscillation frequency *fc S* . In this case, the tracking speed of *ia* is ensured and it would be sufficient to choose the value of *La* with sole consideration given to the inductor current ripple. As the two power switches of AACC operate in a complementary manner, the AACC is operating in continuous current conduction mode. Thus, the duty cycle of *Qa*1 is

$$dQa\ 1\ (t) = 1 - V\text{bus}\ va\ (t)\ . \tag{22}$$

When *Qa*1 is turned ON and *Qa*2 is turned OFF, the voltage across *La* is *V*bus. This voltage causes *ia* to increase. The rippleof *ia* can be expressed as

$$\Delta iLa = V\text{bus}/La \cdot dQa\ 1\ (t) \cdot 1/fsa \tag{23}$$

Substitution of (22) into (23) gives

$$La = (va\ (t) - V\text{bus})\ V\text{bus}/va\ (t)\Delta iLa\ fsa \tag{24}$$

It can be seen from (24) that *La* varies with *va* (*t*) in a oscillation period.

D. Design Example

In this part, an AACC is designed for a cascaded system, as seen in Fig. 9, the system is composed by two phase-shifted full-bridge converters. Table I gives its parameters. In Fig. 9, both the source converter and load converter's voltage regulator are employing a PI controller. In this paper, *fc S*and phase margin of source converter are set at 550 Hz and 45◦, respectively, and *fc L* and phase margin of load converter are set at 5 kHz and 45◦, respectively. According to the circuit and control parameters of the cascaded system, the Bode plots of the source converter's output impedance *Zo* and the load converter's input impedance *Z*in at different loads are plotted in Fig. 10. It can be seen that when the load is lower than 35% full load, *Zo* peak is less than *Z*in , and the cascaded system is stable. Otherwise, there is interaction between *Zo* and *Z*in , the system

Table 1. Circuit Parameters of Source Converter And Load Converter

Source converter (360 V – 48 V 480 W 100 kHz)			
Parameter	value	Parameter	value
Q_1~ Q_4	IRF840	L_{f1}	150 μH
D_{R1}~ D_{R2}	DSEP15-06	C_{f1}	680 μF
Winding Turns Ratio of T_{r1}	5 : 1	L_{r1}	2 μH
K_p	3	K_i	1000
Load converter (48 V – 12 V 480W 100 kHz)			
Parameter	value	Parameter	value
Q_5~ Q_8	IXTP44N10T	L_{f2}	2.2 μH
D_{R3}~ D_{R4}	DSA60C100PB	C_{f2}	4700 μF
Winding Turns Ratio of T_{r2}	3 : 1	L_{r2}	1 μH
K_p	8	K_i	1500

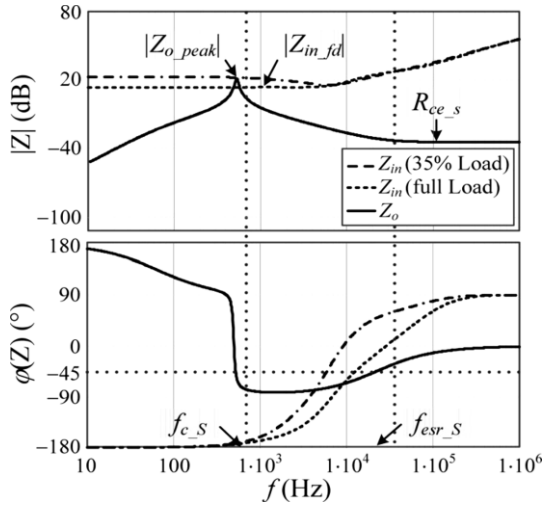

Fig. 10. Impedances of the source and load converters at different loads

Will become unstable, and the AACC is needed. In practice, the impedance characteristics of *Zo* and *Z*in can be measured by a network analyzer without knowing the intrinsic parameters of the subsystems. From Fig. 10, it can be seen that, *Zo* peak = 13.5 Ω, the input impedance of load converter at full load *Z*in *f d* is equal to4.8 Ω, *Rce S* = 0.017 Ω, *fc S* = 550 Hz, and *f*esr *S* = 22.5 kHz. Using (1)–(3) and (7), we can calculate the oscillation angular frequency and *C*bus max, i.e., $\omega = 2\pi fc\ S$ = 3455 rad/s and *C*bus max = 1950 μF. Setting Δ*v*bus allow at 1%*V*bus, the main circuit parameters of AACC can be designed as follows:

1) We choose *Ca* = 20 μF (film capacitors, EACO-STH 200 V/20 μF), then $C*a$ = 20 μF/1950 μF = 0.01.

2) Considering *V*bus = 48 V and (18), *VQa*1 = *VQa*2 =*Va* max 110 V. By (21), *IQa*1 = *IQa*2 = 3 A. Here,FDMS2572 (4.5 A/150V) with *Rds*(ON) of 0.09 Ω isadopted.

3) Considering *fc S* = 550 Hz, *fsa* is chosen as 100 kHz that is much higher than 550 Hz.

4) Setting ΔiL max = 20%$IQa1$ = 0.6 A and from (14) and (24), the curve of minimum value of *La, La* min, in an oscillation period can be plotted in Fig. 11, where the

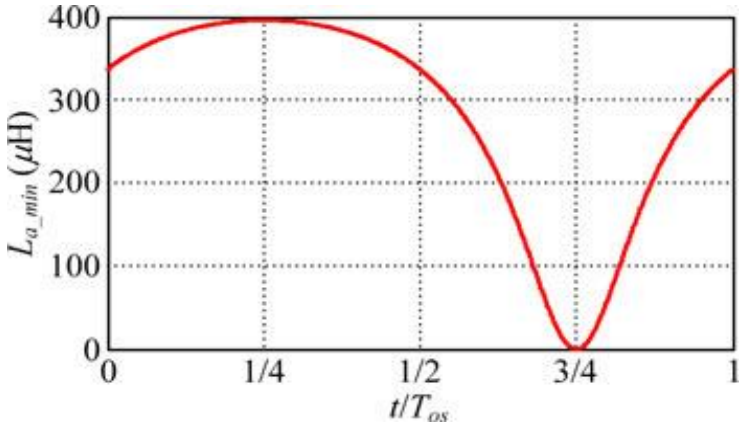

Fig. 11. Plot of the minimal value of *La*

TABLE II: Components of AACC, Passive Capacitor Solution, and the Original cascaded System

Components of AACC			
Main circuit		Control circuit	
Component	Part number	IC	Quantity
Q_{a1}	FDMS2572 (4.5A/150V)	TL074	2
Q_{a2}	FDMS2572 (4.5A/150V)	TL072	1
L_a	NCD EE33/14/13	LM393	1
C_a	EACO-STH 200 V/20 μF	SG3525	1
Components of passive capacitor solution			
Component	Part number		Quantity
C_{bus} (1950 μF)	*Jianghai* CD29S PJ 100 V/390 μF		5
Components of original cascaded system			
Source converter			
Main circuit		Control circuit	
Component	Part number	IC	Quantity
Q_1~ Q_4	IRF840 (8A/500V)	TL074	1
D_{R1}~ D_{R2}	DSEP15-06A (15A/600V)	TL072	1
T_{r1}	NCD EE42/21/20	LM393	3
L_{r1}	NCD EE25/10/7	TLP521-1	1
L_{f1}	NCD EE55/28/25	HCPL3120	4
C_{f1}	*Jianghai* CD294 100 V/680 μF	UCC3895	1
Load converter			
Main circuit		Control circuit	
Component	Part number	IC	Quantity
Q_5~ Q_8	IXTP44N10T (44A/100V)	TL074	1
D_{R3}~ D_{R4}	DSA60C100PB (60A/100V)	TL072	1
T_{r2}	NCD EE42/21/20	LM393	3
L_{r2}	NCD EE25/10/7	TLP521-1	1
L_{f2}	NCD EE42/21/20	HCPL3120	4
C_{f2}	*Jianghai* CD294 50 V/4700 μF	UCC3895	1

Maximum value of *La* min is 395 μH. Here, we choose *La* = 395 μH. Considering the cost is a matter of concern in practical, Table II lists the selected components of AACC, passive capacitor solution, and the original cascaded system. Currently, the cost of AACC is slight higher than the passive capacitor solution, and accounts for about 9% of the original cascaded system.

5 Experimental Verification

In order to verify the validity of the proposed AACC, a prototype has been built and tested. The parameters of the prototype have been given in Section IV-D. Fig. 12 shows the steady-state experimental waveforms of the source converter and load converter operating individually. Fig. 13(a) and (b) shows the individual dynamic waveforms of the source and load converters when their load steps between full load and 10% full load, respectively. As seen from the figures, both source and load converters are stable and working well.

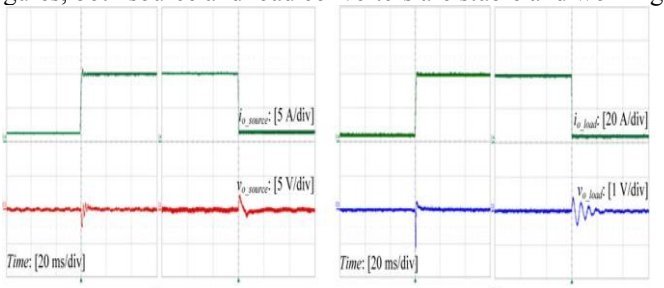

Fig. 12. Individual dynamic waveforms of the source and load converters when their load steps between full load and 10% full load:
(a) source converter and (b) load converter

Considering that the cascaded system can be stable with a 1950 μF passive capacitor (Cbus max) or AACC in the full load range. Fig. 18 compares their dynamic performance when the load steps between full load and 10% full load. It shows that the system with AACC has a faster dynamic response than that of the system using the passive capacitor solution. According to the reason can be explained as follows. The equivalent capacitor of AACC is adaptively varied by the load. Its value is always smaller than 1950 μF and approaches zero when the system is stable. And a smaller Cbus, of course, means a faster dynamic performance for the cascaded system. In addition, compared with Figs. 13 and 18(b), it seems that the cascaded system with AACC has a similar dynamic performance with its individual subsystems.

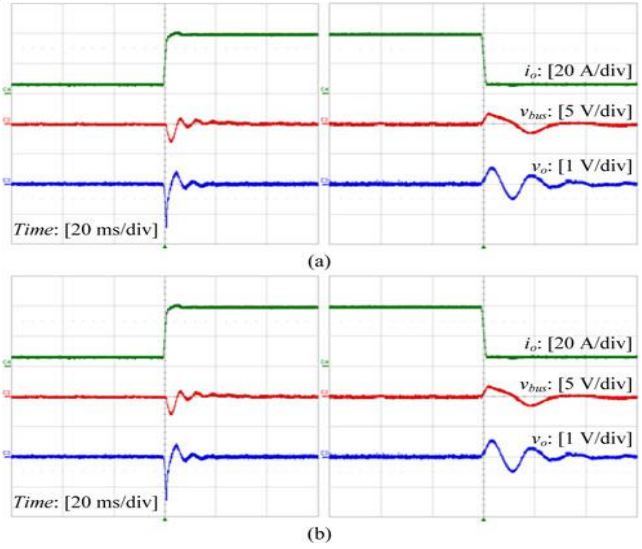

Fig. 13. Waveforms of cascaded system when the load steps between full load and 10% full load: (a) with the AACC (b) without the AACC

6 Conclusion

When the AACC is a good suggests that to resolve the instability downside of the dc distributed power supply. In the presents days they will offers the AACC as identical adjective bus capacitance will be changeable per then the cascaded system have their output power, so we can avert the electrical resistance can communicate to the cascaded system with the quantity of the output electrical resistance in the supply convertor. Betting in the edge of the undisturbed conditions in the cascaded system, therefore the AACC is adjectively functionaries. Once the move in the cascaded system was broad in the AACC supply to the additional power of the produce to the bigger importance capacitance. Once they can moves in the cascaded system have a very small value, when the AACC can supply less power in the produce have smaller importance capacitance. They will tally in the present technique, the projected convertor solely has they discover the cascaded system to the bus voltage while not dynamic something in the present subsystems, thus they will be a stylish to the customary can be measuring in the dc DPS. Then AACC will been ascertain carefully see the power values that is four thousand eight hundred zero watts and we can see different voltage ratings in the cascaded system. After we can see the exacta output results of the experimental in the validity of the analysis.

References

[1]. F. Blaabjerg, A. Consoli, J. A. Ferreira, and J. D. van Wyk, “The future of electronic power processing and conversion,” *IEEE Trans. Power Electron.*, vol. 20, no. 3, pp. 715–720, May 2005.

[2]. J. D. van Wyk and F. C. Lee, “Power electronics technology—Status and future,” in *Proc. CPES*, 1999, pp. 61–70.

[3]. Nagarjuna, A., Suresh Kumar, T., Yogeswara Reddy, B., Udaykiran, M., Fifteen level cascaded H-bridge multilevel inverter fed induction motor, International Journal of Innovative Technology and Exploring Engineering, 2019, 8(11), pp. 640–645.

[4]. K. T. Kornegay, “Design issues in power electronic building block (PEBB) system integration,” in *Proc. IEEE VLSI*, Apr. 1998, pp. 48–52.

[5]. T. Ericsen, “Power electronic building blocks—A systematic approach to power electronics,” in *Proc. IEEE Power Eng. Soc. Summer Meeting*, 2000, pp. 1216–1218.

[6]. B. J. Varghese, P. B. Bobba and M. Kavitha, "Effects of coil misalignment in a four coil implantable wireless power transfer system," 2016 IEEE 7th Power India International Conference (PIICON), Bikaner, India, 2016, pp. 1-6

[7]. D. Boroyevich, I. Cvetkovi c, D. Dong, R. Burgos, F. Wang, and F. C. Lee, “Future electronic power distribution systems—A contemplative view,” in *Proc. IEEE OPTIM*, May 2010, pp. 1369–1380.

[8]. S. Luo, “A review of distributed power systems part I: DC distributed power system,” *IEEE Aerosp. Electron. Syst. Mag.*, vol. 20, no. 8, pp. 5–16, Aug. 2005.

[9]. B. J. Varghese and P. B. Bobba, "Design and analysis of a robust system for wirelessly powering implantable devices," 2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), Delhi, India, 2016, pp. 1-5,

[10]. Raju, N.A., Suresh Kumar, T., Forward converter based switch mode power supply with modified boost converter as PFC, International Journal of Innovative Technology and Exploring Engineering, 2019, 8(11), pp. 3860–3864.

[11]. L. R. Lewis, B. H. Cho, F. C. Lee, and B. A. Carpenter, “Modeling, Analysis and design of distributed power systems,” in *Proc. IEEE PESC*, Jun. 1989, pp. 152–159.
[12]. Karthik Rao, R., Bobba, P.B., Suresh Kumar, T., Kosaraju, S., Feasibility analysis of different conducting and insulation materials used in laminated busbars, Materials Today: Proceedings, 2019, 26, pp. 3085–3089.
[13]. G. A. Franz, G. W. Ludwig, and R. L. Steigerwald, “Modeling and simulation of distributed power systems,” in *Proc. IEEE PESC*, 1990, pp. 606–610.
[14]. S. Schulz, B. H. Cho, and F. C. Lee, “Design considerations for a distributed power system,” in *Proc. IEEE PESC*, 1990, pp. 611–617.
[15]. B. H. Cho and B. Choi, “Analysis and design of multi-stage distributed power systems,” in *Proc. Int. Telecomm. Energy Conf.*, Kyoto, Japan, Nov. 1991, pp. 220–226.
[16]. M. Kavitha, P. B. Bobba and D. Prasad, "Effect of coil geometry and shielding on wireless power transfer system," 2016 IEEE 7th Power India International Conference (PIICON), Bikaner, India, 2016, pp. 1-6,