Comparison Analysis of Semiconductor Characterisation topologies using Energy Recirculation Concept

Bobba Phaneedra Babu[1*], *Allem Rama Krishna* Reddy[1], *Gujjula* Pratap[1] , *Murra* Harshavardhana Reddy[1], *A. Hussien* Abbas[2], *Raj* Kumar[3], *J.*Praveen[1]
[1]EEE Department, GRIET, Hyderabad, Telangana
[2]Computer Technical Engineering Department, College of Technical Engineering, The Islamic University, Iraq
[3]Uttaranchal School of Computing Sciences, Uttaranchal University, Dehradun 248007 INDIA

Abstract: Energy recirculation concept in semiconductor device characterization can increase power handling capacity of the source and it will reduce naturally existing high electrical stresses on device under test. The proposed energy recirculation and storage circuits (ERSC) can be employed as a device in-situ testing unit, by storing and recirculating the energy of the storage elements. ERSC enables devices to be checked at full-power pressures without being attached to a high-power load or requiring high power source. ERSC has four active states of operations achieved by the two active switches of the proposed converter. This converter can function in four different modes of operation, namely - soft start, magnetize, charge, and energy recirculation modes. Another advantage of this converter is that the two circuits can be constructed to work synchronously or asynchronously, allowing for the testing of faster or slower devices depending on the performance of the device being tested. In this paper double pulse test, single ended buck boost and cascaded boost -buck ERSC converters are simulated using MATLAB/SIMULINK and based on the results cascaded boost-buck ERSC having better performance compared to existing testing methods.

1. Introduction

This paper shows that we can test the high-power devices with low voltage/current sources by using ERSCs. The concept of "recirculating energy" has a considerably broader application, and it can be utilised to design a new family of converters for power-factor

* Corresponding Author: bobbaphani@gmail.com

correction, capacitor charging, and bi-directional power transmission. Increasing transitory reaction, for example. The concept is basic in that it explains how to accomplish something by offering a second conduit for power flow, a second degree of freedom in control. The notion is applied to buck and boost derived topologies in this study to demonstrate the evolution of a family. Energy Recirculation and Storage Circuits are two types of circuits (ERSCs). This document, which outlines recent research and discusses the evolution of connection rules to construct an ERSC; state equations for the converter family; a comprehensive family of single- and double-ended circuits .This document, which outlines recent research and discusses the evolution of connection rules to construct an ERSC; description and verification of an ideal boost/buck derived ERSC's operation, and application to power systems correction of factors This does not contain the extension to resonant topologies.

In this paper we have presented working methods of double pulse test, single ended buck/boost ERSC and cascaded boost/buck ERSC in section2 and the simulation results of this circuits are discussed in the section 3, conclusion and scope are mentioned in section 4 and 5 respectively.

2 Methodology

The Energy recirculation devices are used for producing high source from that we used ERSC circuit for testing the semiconductor characteristics. Based on switching, efficiency, and analysis, we considered three circuits on testing the semiconductor devices. Double pulse circuit, Single cascaded boost/buck circuit and cascaded boost/buck circuit.

2.1 Double pulse test (DPT):

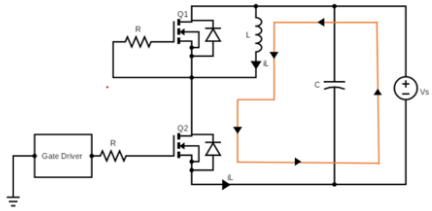
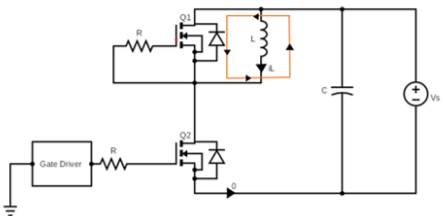
Switch State Topologies	Operation	State Equation
	When Q2 is on inductor L stores the magnetic energy.	$\frac{di_L}{dt} = \frac{V_s}{L}$
	When Q2 is off, current flows as shown path.	$\frac{di_L}{dt} = 0$

Fig.1. Operation states of DPT

The double pulse test, often referred to as the double pulse technique [2] or double pulse method, is an experimental technique used in electronics and power electronics to investigate

the behaviour of electronic devices, especially power semiconductors like transistors and diodes.

The double pulse test's objective is to evaluate a power semiconductor device's performance and switching characteristics under particular operating circumstances. It entails delivering the gadget with two closely spaced electrical pulses and monitoring its reaction.The first pulse, sometimes referred to as the "trigger" or "commutation" pulse, typically transforms the device quickly from one state (ON) to another state (OFF), or vice versa. The trigger pulse is followed by a longer-duration pulse known as the "main" or "load" pulse, which reflects the usual operating current or voltage circumstances.

There two switch states possible in double pulse test. The switch states and the state equations are provided in the figure 1. Here Q_1 is a free-wheel MOSFET whereas Q2 is a gate driven MOSFET.

In double pulse test first, we need to get a desired test current to test the DUT, which can be obtained by turning on the Q_2 for long duration and the current flow is shown in the figure 1. This is the first step in double pulse test. After achieving desired testing current, second step is turn-off the pulse for short duration, so that we maintain test current as constant. After this step, one more pulse is applied on the device. This pulse helps to get the turn off and turn on characteristics of the switching device and other parameters.

Simulation of the double pulse test is done using MATLAB software and the MATLAB connection blocks are shown in the figure 2. Here the gate pulse is triggered using the controller and the device which is under test is placed inside the DUT block and the results are discussed in the chapter 3 under section 3.1.

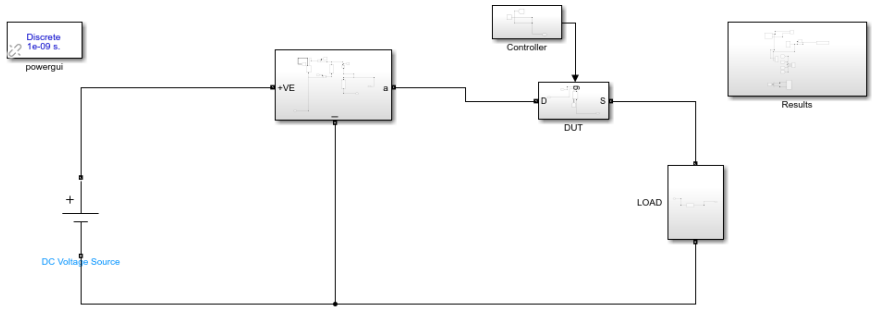


Fig.2. MATLAB circuit of double pulse test

2.2 Single ended buck/boost:

Single ended buck/buck is an energy recirculate and storage circuit [1][3-4]. There are two modes of operation for the single-ended buck/boost ERSC, depicted in figure 3. The modes allow the circuit to charge the feedback capacitor to high voltage levels while the peak input current is constrained to the maximum current capability of the power-limited input voltage source.

It should be moted that there is only one active switch with two state variables in the circuit. So, we can control one state variable as constant with the help of modulation of the switch. Here we control the magnetizing inductor current constant between upper and lower ripple specifications, while the feedback capacitor voltage was allowed to increase.

The two modes of operation designed for the single-ended buck/boost ERSC are magnetize mode and charge mode. The magnetize mode is used as a “start-up” mode where the magnetizing inductor current,i_L, is increased from zero to the peak output current, while the voltage across the feedback capacitor is held constant with an AC ripple at some low DC pre-charge voltage. The charge mode commences once the maximum output current from the

input voltage source is reached during the start-up magnetize mode. The charge mode is used to charge the feedback capacitor to high voltage levels while holding the magnetizing inductor near to constant. This mode is the "main" mode of operation which the circuit is designed.

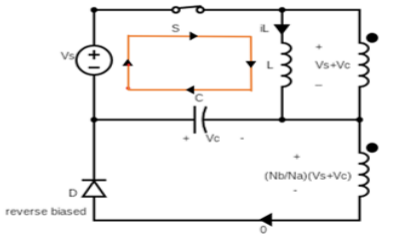
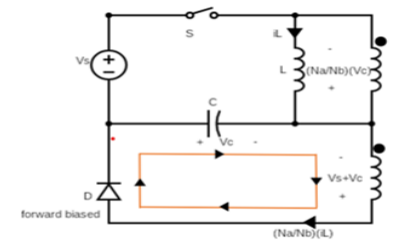
Switch State Topologies	Operation	State Equation
	Increase the inductor current i_L and decrease the voltage across capacitor	$\frac{di_L}{dt} = \frac{V_s + V_c}{L}$ $\frac{dV_c}{dt} = \frac{-i_L}{C}$
	Charge the capacitor to the upper pre charge voltage and the direction of current flow as shown	$\frac{di_L}{dt} = \left(\frac{-V_c}{L}\right)\left(\frac{N_a}{N_b}\right)$ $\frac{dV_c}{dt} = \left(\frac{i_L}{C}\right)\left(\frac{N_a}{N_b}\right)$

Fig.3. Operation states of single ended cascade buck/boost ERSC

Simulation of the single ended buck/boost ERSC is done using MATLAB software and the MATLAB connection blocks are shown in the figure 4. Here the gate pulse is triggered using the controller and the device which is under test is placed inside the DUT block and the results are discussed in the chapter 3 under section 3.2. Here the energy is recirculated using a feedback capacitor which works on constant-voltage technique.

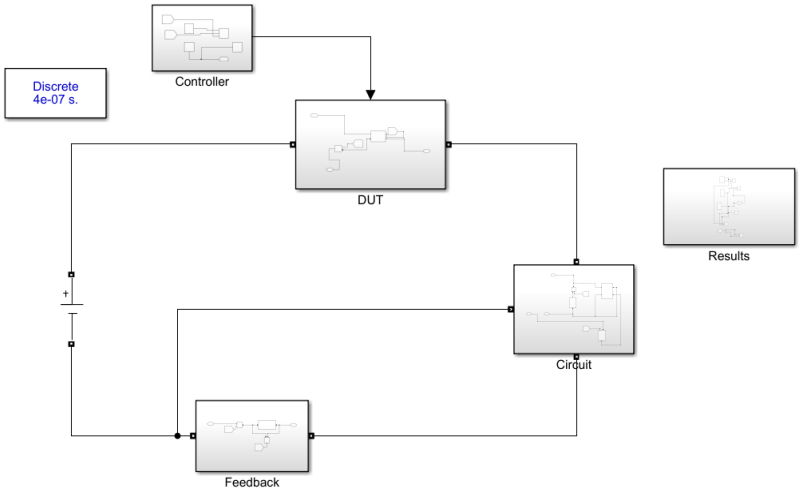


Fig.4. MATLAB circuit of single ended buck/boost ERSC

2.3 Cascaded boost/buck ERSC:

The ideal cascaded boost/buck ERSC, has three state variables: [1][3-4]effective current source inductor current, voltage across the energy buffer capacitor, and feedback inductor current. Cascaded topologies, as opposed to single-ended topologies, have four active switch states that control energy storage in the feedback and buffer elements, as well as the filter element associated with an effective input source. Figure 5 includes state equations for all four switching states.

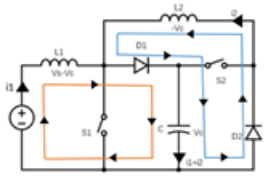
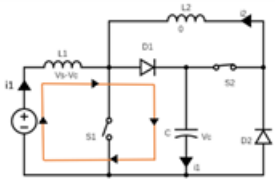
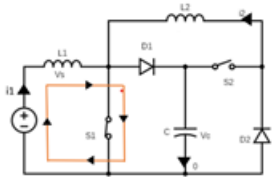
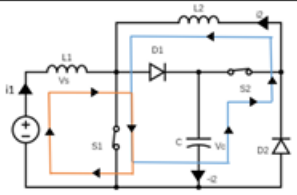
Switch State Topologies	Operation	State Equation
	Capacitor get charged to maximum voltage and the change in feedback energy is decrease with charge in capacitor.	$\frac{di_1}{dt} = \left(\frac{1}{L_1}\right)(V_S - V_C)$ $\frac{dV_C}{dt} = \left(\frac{1}{C}\right)(i_1 + i_2)$ $\frac{di_2}{dt} = \left(\frac{1}{L_2}\right)(-V_C)$
	Capacitor get charged as in current path and change in feedback current is zero.	$\frac{di_1}{dt} = \left(\frac{1}{L_1}\right)(V_S - V_C)$ $\frac{dV_C}{dt} = \left(\frac{1}{C}\right)(i_1)$ $\frac{di_2}{dt} = 0$
	Input inductor current increases to maximum and the capacitor voltage remains same.	$\frac{di_1}{dt} = \left(\frac{1}{L_1}\right)(V_S)$ $\frac{dV_C}{dt} = 0$ $\frac{di_2}{dt} = 0$
	Input inductor current increases to maximum and the capacitor gets discharged through feedback path.	$\frac{di_1}{dt} = \left(\frac{1}{L_1}\right)(V_S)$ $\frac{dV_C}{dt} = \left(\frac{1}{C}\right)(-i_2)$ $\frac{di_2}{dt} = \left(\frac{1}{L_2}\right)(V_C)$

Fig.5. Operation states of cascaded boost/buck ERSC

For the ERSC, three modes of operation are being investigated. The modes enable controlled energy storage in all three elements. Soft-Start is the first mode, which regulates the build-up of current, i_1, in the input filter inductor and voltage, V_c, across the buffer capacitor. The Charge Mode, which controls the charging of the buffer capacitor to a pre-set voltage, V_c, is the second mode. During this time, all input energy is transferred to the buffer capacitor. The circuit enters the magnetise mode when the capacitor is charged to V_c. This is the primary mode of operation intended for the circuit. While i_1 and V_c are held constant within a ripple bound, the feedback inductor current, i_2, increases to high current levels.

Simulation of the single ended buck/boost ERSC is done using MATLAB software and the MATLAB connection blocks are shown in the figure 6. Here the gate pulse is triggered

using the controller which is a closed loop control whereas single ended buck/boost is a open loop control and the device which is under test is placed inside the DUT block and the results are discussed in the chapter 3 under section 3.3. Here the energy is recirculated using a feedback capacitor which works on constant-voltage technique.

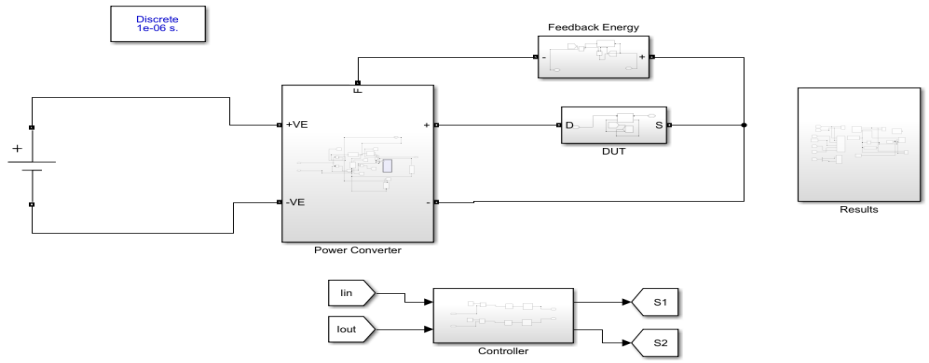


Fig.6.MATLAB circuit of cascaded boost/buck ERSC

3 Simulation Results and Discussion

The mathematical model of above discussed circuits is simulated using MATLAB software. Without considering the losses of all the elements in the model we cannot achieve proper results. Hence to represent all the losses non-ideal circuit is simulated, and its circuit diagram is shown below, by considering all the parasitic elements. The simulation parameters of switch are mentioned in figure 7. Here we considered the values of SiC (silicon carbide) as a testing device.

Parameter	Rated Values
Maximum voltage	1500V
Maximum current	50A
On-state resistance	200mΩ
Forward voltage	1.5V
Threshold voltage	5V

Fig.7. Device parameters

3.1 Double pulse test:

Double pulse test circuit is simulated in MATLAB using a 1000V power supply which is capable of delivering a power of 25KW. During the DPT, the power delivered by the battery to the circuit can be analysed. This power is a function of the voltage across the switch and the current flowing through it. As the switch turns on, the battery delivers power to the circuit, as shown in the below graphs. Power losses during the testing is also shown in the same

graph, from this graph power loss during a testing of single device is nearly 50percent of the input power supply.

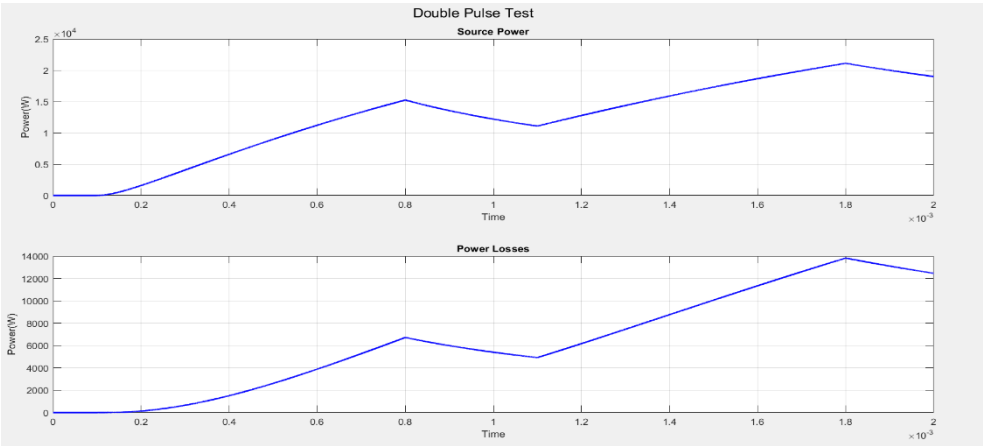


Fig.8. Performance analysis of Double pulse test

V-I characteristics of the DUT during the switch on and off state is shown in figure 9. During switch turn-on, the voltage across the switch decreases from its initial off-state voltage to a lower on-state voltage. At the same time, the switch current rises from zero to a steady-state current level. This transition is typically associated with the charging of parasitic capacitances and the reduction of the effective resistance within the switch. During switch turn-off, the voltage across the switch rises from its on-state voltage to a higher off-state voltage. Simultaneously, the switch current decreases from the steady-state value to zero. This transition involves the discharge of parasitic capacitances and the increase in the effective resistance within the switch.

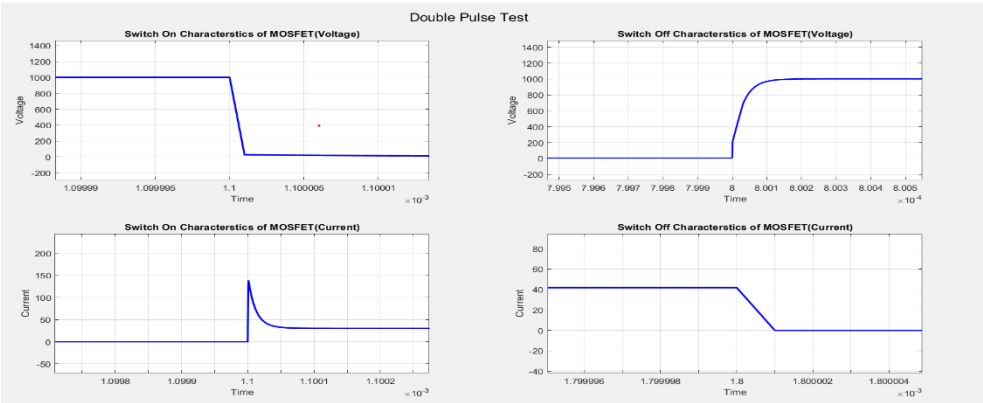


Fig.9. Characteristics of DUT in double pulse test

By analysing these voltage-current characteristics during switch on and off, you can gain insights into the switch's performance, including its switching speed, transient behaviour, and power dissipation characteristics.

3.2 Single cascaded boost/buck:

The single ended cascaded Boost/Buck ERSC circuit [5-7]. is simulated to obtain the same characteristics of the DUT similar to the double pulse test. The difference between those two is here we use a low voltage power source. For our simulation we considered a voltage source of 200V and capable of delivering 1.4KW power to the circuit. This circuit works on energy recirculation as discussed in section 2. The single-ended buck/boost ERS converter operates by utilizing energy recovery techniques to achieve high efficiency. By intelligently controlling the switch's operation, the converter can effectively transfer energy between the input and output sides while minimizing losses. The below figure shows the power delivered by the battery and the power losses in the circuit and the last column shows the energy circulated in the feedback capacitor during the simulation time.

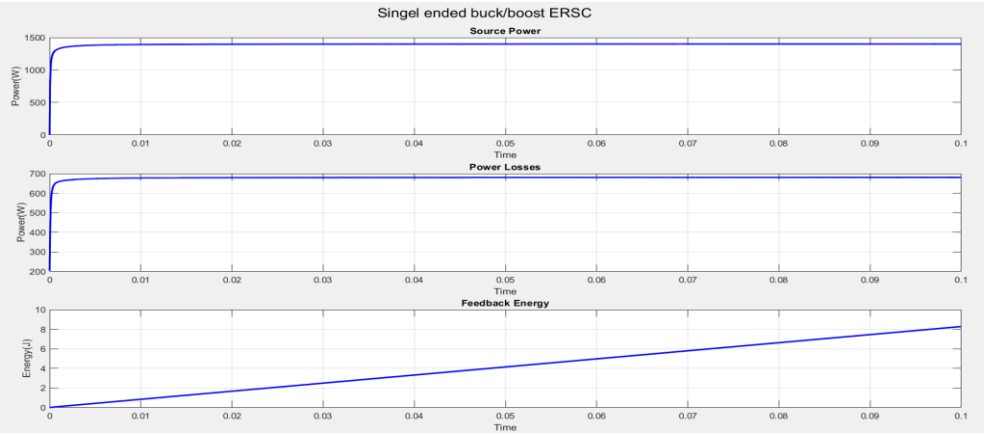


Fig.10. Performance analysis of single ended buck/boost ERSC

3.3 Cascaded boost/buck ERSC:

Cascaded boost/buck ERSC is similar circuit to the single ended buck/boost [5-7]. Here also we use the concept of energy recirculation. Without considering losses of all the elements of ERSC, total losses of the converter, the circuit would not proceed to go to operate in the last mode called energy recirculation, where all the states of energy stored elements are remains unaltered while the input source provides power to compensate the losses in the circuit. Hence to represent all the losses non-ideal proposed ERSC is simulated, and its circuit diagram is shown in below figure, by considering all the parasitic elements. To investigate the dynamic and steady state characterization of DUTs using proposed ERSC, simulation-based analysis is carried out on the MATLAB Simulink environment.

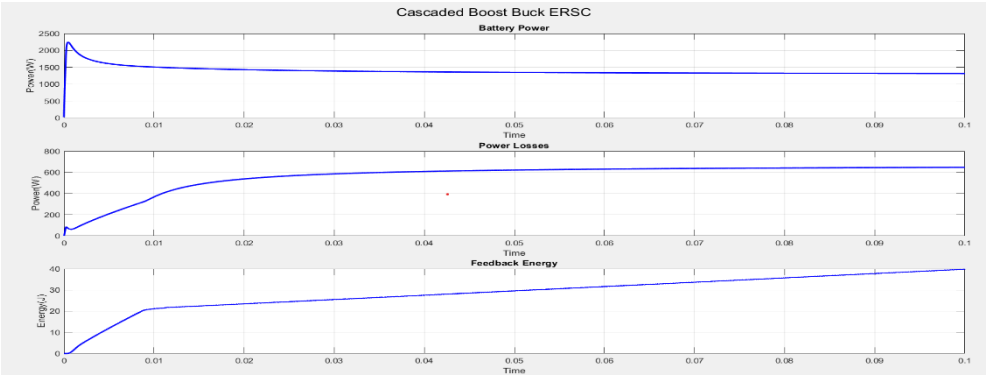


Fig.11. Performance analysis of Cascaded boost/buck ERSC

The results obtained from the simulation and analysis of the cascaded boost/buck energy recirculation converter reveal valuable insights into its performance. The simulation focused on evaluating the power delivered by the converter, the power losses within the circuit, and the energy feedback mechanism. The converter demonstrated efficient power delivery, enabling voltage stepping up or stepping down as required. The power losses within the circuit, including switching and resistive losses, were analysed to optimize the converter's efficiency. Moreover, the energy feedback mechanism was examined to ensure effective utilization of energy and minimize wastage. These results provide a comprehensive understanding of the cascaded boost/buck energy recirculation converter's performance and contribute to its improved design and application in various power electronic systems.

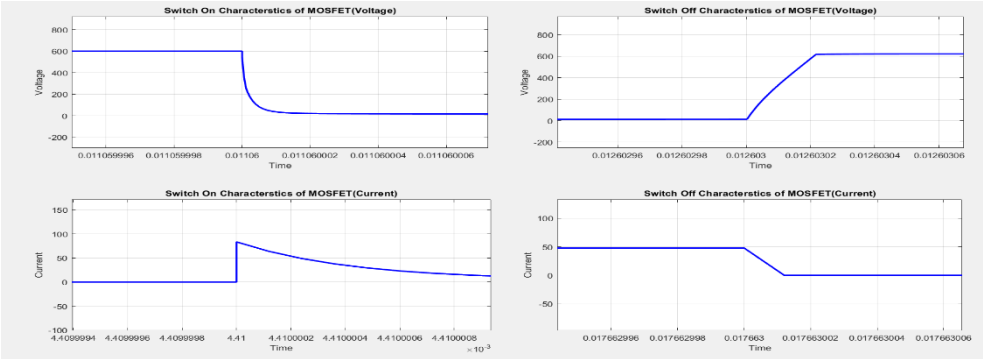


Fig.12. Characteristics of DUT in cascaded boost/buck ERSC

The graph representing the power delivered by the battery will show a curve that corresponds to the switch's on and off states. Initially, the power delivered will be low, close to zero, as the switch is off and there is no current flowing. As the switch turns on, the power delivered by the battery increases and reaches a steady-state value. During turn-off, the power delivered decreases back to zero. By analysing the power delivered by the battery and the power losses during the DPT, you can assess the efficiency of the switch and identify areas for improvement in terms of reducing power losses and optimizing the overall system performance.

4 Conclusion

From the simulation results as shown in section 3, for the double pulse test in the context of in-situ testing of semiconductor devices have shed light on the substantial power wastage associated with conventional testing methods. This highlights the pressing need for an improved approach that can mitigate this problem. To address this challenge, an effective method for utilizing energy recirculation and storage circuits has been proposed.

Through the simulation of two different circuits using MATLAB/SIMULINK, valuable insights have been gained regarding their energy recirculation capabilities. The first circuit, the single-ended buck/boost ERSC, demonstrated the ability to recirculate a relatively smaller amount of energy compared to the second circuit, the cascaded boost/buck ERSC. This performance comparison offers valuable information for optimizing energy utilization during in-situ testing of semiconductor devices.

The integration of energy recirculation and storage circuits in in-situ testing of semiconductor devices has the potential to significantly reduce power wastage. By implementing this approach, energy efficiency can be enhanced, leading to improved testing methodologies and more sustainable practices in semiconductor device manufacturing. This advancement can ultimately contribute to reduced energy consumption, increased operational efficiency, and environmental conservation.

In summary, the findings from this MATLAB/SIMULINK simulation indicate that the use of cascaded boost/buck ERSC presents a better alternative to the conventional double pulse test and single ended buck/boost ERSC in the in-situ testing of semiconductor devices. Further research and development in this area can pave the way for the implementation of more efficient and eco-friendly testing strategies, enabling the semiconductor industry to achieve higher levels of performance, reliability, and sustainability.

Acknowledgement

Authors would like to thank Department of Science & Technology (Technology Development & Transfer – Device Development Programme), Ministry of Science & Technology, Govt. of INDIA and GRIET Management for financial support of this work. Grant Number: DST/TDT/DDp-39/2021 (G) dt: 11 Feb 2022.

References

1. D. C. Hopkins and D. W. Root, *Synthesis of a new class of converters that utilize energy recirculation* Proceedings Power Electronics Specialist Conference Taiwan (1994)
2. S. S. Ahmad and G. Narayanan, *"Double pulse test based switching characterization of SiC MOSFET,"* National Power Electronics Conference (NPEC), Pune, India, (2017)
3. R. W. Root, Jr., *Synthesis of Switch-Mode Power Electronic Circuits for Energy Recirculation and Storage*, Master's Thesis – Auburn University (1993).
4. J. Srinivas Rao, Suresh Kumar Tummala, Narasimha Raju Kuthuri, Comparative investigation of 15 Level and 17 level cascaded h-bridge MLI with cross h-bridge MLI fed permanent magnet synchronous motor, Indonesian Journal of Electrical Engineering and Computer Science, 21(2), pp: 723-734, (2020)
5. Kosaraju, S., Anne, V.G. & Popuri, B.B. Online tool condition monitoring in turning titanium (grade 5) using acoustic emission: modeling. Int J Adv Manuf Technol 67, 1947–1954 (2013).
6. Satyanarayana Kosaraju, Swadesh Kumar Singh, Tanya Buddi, Anil Kalluri & Ahsan Ul Haq (2020) Evaluation and characterisation of ASS316L at sub-zero temperature, Advances in Materials and Processing Technologies, 6:2, 365-375
7. S. Singer, *"The Application of "Loss-Free Resistors" in Power Processing Circuits,"* (1989)
8. Tummala, S.K., Indira Priyadarshini, T., Morphological Operations and Histogram Analysis of SEM Images using Python, Indian Journal of Engineering and Materials Sciences, 2022, 29(6), pp. 794–798.
9. R. D. Middlebrook and S. Cuk*, "Modelling and Analysis Methods for DC-to-DC Switching Converters,"* (1977)
10. Raju, N.A., Suresh Kumar, T., Forward converter based switch mode power supply with modified boost converter as PFC, International Journal of Innovative Technology and Exploring Engineering, 2019, 8(11), pp. 3860–3864.
11. R. D. Middlebrook and S. Cuk*, "A General Unified Approach to Modelling Switching-Converter Power Stages,"* (1976)
12. Suresh Kumar Tummala, Phaneendra Babu Bobba & Kosaraju Satyanarayana (2022) SEM & EDAX analysis of super capacitor, Advances in Materials and Processing Technologies, 8:sup4, 2398-2409

13. Satyanarayana, K., Gopal, A.V., Babu, P.B., Design optimisation of machining parameters for turning titanium alloys with taguchi-grey method, International Journal of Machining and Machinability of Materials, 2013, 13(2-3), pp. 191–202
14. K. H. Liu and F. C. Lee, "*Topological Constraints on Basic PWM Converters,* " Proc. of the IEEE Power Electronics Spec, Japan (1988)
15. Prasad, K.S., Gupta, A.K., Singh, Y., Singh, S.K., A Modified Mechanical Threshold Stress Constitutive Model for Austenitic Stainless Steels, Journal of Materials Engineering and Performance, 2016, 25(12), pp. 5411–5423
16. Singh, S.K., Tambe, S.P., Raja, V.S., Kumar, D., Thermally sprayable polyethylene coatings for marine environment, Progress in Organic Coatings, 2007, 60(3), pp. 186–193.