Performance analysis of Ternary Adder and Ternary Multiplier without using Encoders and Decoders

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Abstract: This work presents comparison of ternary combinational digital circuits that reduce energy consumption in low-power VLSI (Very Large Scale Integration) design. CNTFET and GNRFET-based ternary half adder (THA) and multiplier (TMUL) circuits has been designed using ternary unary operator circuits at 32nm technology node and implement two power supplies Vdd and Vdd/2 without using any ternary decoders, basic logic gates, or encoders to minimize the number of used transistors and improve the energy efficiency. The effect of CNTFET and GNRFET parametric variation with threshold voltage on performance metrics namely delay and power has been analyzed. Dependence of threshold voltage on the geometry of carbon nanotube and graphene nanoribbon makes it feasible to be used for ternary logic design. It is analyzed that CNTFET based circuits are energy efficient than the GNRFET- based circuits. It is also concluded that the CNTFET-based circuitshas less power-delay product (PDP) when compared to GNRFET- based circuits. CNTFET-based THA is 23.5% more efficient than GNRFET-based THA and CNTFET-based Tmul is97.8% more efficient than GNRFET-based Tmul.All the digital circuits have been simulated using HSPICE tool.
Keywords: Carbon nano-tube field effect transistors (CNTFET),Graphene nano-ribbon field effect transistors(GNRFET), Ternary logic circuits, unary operators.

1. Introduction

CMOS is one of the most used semiconductor device in low-power VLSI design. However, we can observe short channel effects that increases the leakage currents and

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power dissipation complications in small chips. Due to this many scientists proposed various alternative solutions in the transistor technologies like FinFET (Fin Field-Effect Transistor), Spin-wave, Single-electron devices, CNTFET,GNRFET. Among all different transistor technologies, CNTFET and GNRFET has a higher performance. The CNTFET and GNRFET model includes the various parameters such as the allocation of carbon transmit speed and better mobility, then, it can be appropriate to various alternative circuits[1-6]. It can also used in integrated circuits and it can cause low voltage, which results in lower power consumption. The CNTFET structure uses CNT as a channel in between source and drain terminals similar to conventional CMOS structure which is shown in Figure 1[7-12]. The GNRFET structure uses GNR as a channel in between source and drain terminals similar to conventional CMOS structure which is shown in Figure 4.The binary circuits require high energy consumption. Whereas, MVL circuits reduce the consumption of energy because the MVL digit can hold over two states of data.

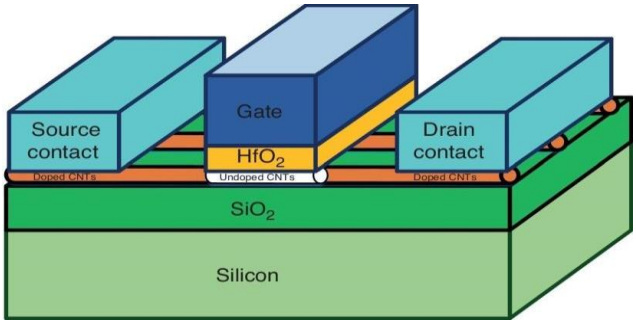

Fig 1. Structure of CNTFET

The ternary unary operators, CNTFET transistor, transmission gates and applies dual-voltages (Vdd, Vdd/2) in the designs to decrease the PDP of the proposed TFA(Ternary Full Adder). This technique is used to save battery consumption.

GNRFET (Graphene nano-ribbon field effect transistors)

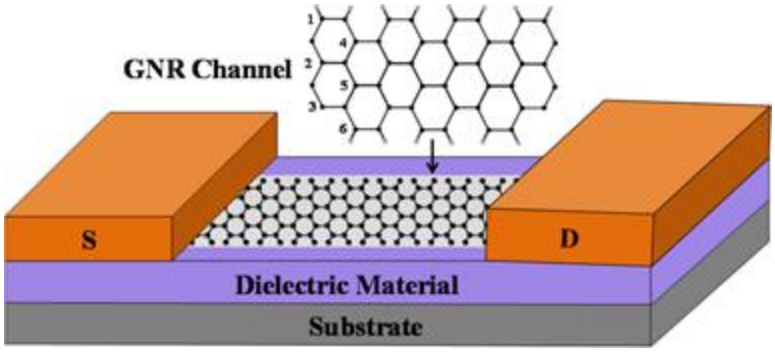

Fig 2. Structure of GNRFET

The structure of GNRFET looks like similar to the traditional MOSFET which is shown in Figure 4. The GNRFET consists of four terminals with gate, drain, source and bulk

terminals. In which undoped GNRs are placed under the gate terminal while heavily doped placed under source and drain terminals[14-20]. The device on and off conditions are based on the potential available at the gate terminal. The V-I characteristics of GNRFET are also same as conventional MOSFET.

The width (W) of GNR is calculated as

$$W = (N + 1)\frac{\sqrt{3}}{2}a \quad (1)$$

Where, 'N' represents no of dimer lines which is proportional to width of GNR, a is the lattice constant i.e., 0.142 nm. The dimer lines are inversely proportional to band gap of GNR. The voltage that is required to turn ON the FET is called as threshold voltage. The threshold voltage of GNRFET is inversely proportional to the width of GNR and is given as below

$$Vth = Eg3\mathrm{e} \quad (2)$$

Where, $Eg = 2|\alpha|\Delta E$ is the band gap and e is the unit electron charge. α=0.27 for N=3P; α=0.4 for N=3P+1; α=0.066 for N=3P+2, $\triangle E = \frac{h v_{\mathbf{F}} \Pi}{W}$, ħ = 6.5821 × 10^{-16}, $v_{\mathbf{F}}$ =10^6 .

For the dimer lines 6 the width of GNR is 0.86 nm and the threshold voltage is 0.43 V from (2). The width of GNR is calculated by dimer lines N using (1). The dimer lines of GNR increases as the width increases and the dimer lines is inversely proportional to band gap. GNRFETs provide equal opportunity to control threshold voltage by altering the width of GNR. We use multi width GNRFET design for ternary logic implementation[21-24]. The Stanford GNRFET SPICE model is used for simulating the GNRFET based ternary logic gates. This is a SPICE model developed for unipolar, MOSFET-like GNRFET devices and it depends on the presumption of ballistic transport, which is just precise in a short channel GNRFET. In addition, it represents accurate and companionable GNRFET configurations for HSPICE simulations [14- 16]. This paper presents the brief introduction to CNTFET and GNRFET in section 1.Ternary gates are discussed in Section 2. Proposed GNRFET -based THA and Tmul circuits in Section 3.Finally section 4 concluded this work.

Proposed designs and simulations:

In this work, the circuits are designed by using CNTFETs .In CNTFETs the threshold voltage depends on the carbon nano-tube (CNT) diameter by the following equation,

$$Vth = \frac{0.43}{Dcnt} \quad (3)$$

Where Dcnt is the CNT diameter.

This proposed circuits have 2 diameter CNTs, where D1=1.487 nm and D2=0.783nm.The operation of the CNTFET and GNRFET Transistor, and the relation between the threshold voltage and the CNT diameter and Dimer Lines is in Table 9.

Table 1. CNTFET and GNRFET simulation parameters

Type	**Diameter**	**Threshold Voltage**	**Dimer Lines (n)**	**Voltage Gate** **0V**	**0.45V**	**0.9V**
P	D1	-0.289V	12	ON	ON	OFF
	D2	-0.559V	7	ON	OFF	OFF
N	D1	0.289V	12	OFF	ON	ON
	D2	0.559V	7	OFF	OFF	ON

Ternary Half Adder

A ternary half adder is a digital Circuit that performs addition of two ternary (base-3) digits, resulting in a sum digit and carry digit. The truth table is as shown in Table 10.

Table 2. Truth table of Ternary Half Adder

A	**B**	**CARRY**	**SUM**
0	0	0	0
0	1	0	1
0	2	0	2
1	0	0	1
1	1	0	2
1	2	1	0
2	0	0	2
2	1	1	0
2	2	1	1

Themathematical expression of sum and carry for ternary half adder can be obtained from Table 2 are given below.

$SUM= 2.\ (A_0B_2 + A_1B_1 + A_2B_0) + 1.\ (A_0B_1 + A_1B_0 + A_2B_2)$

$CARRY= 1.\ (A_1B_2 + A_2B_1 + A_2B_2)$

The above truth table can be also represent as shown in Table 11.

Table 3. Modified Truth table for sum and carry

Sum

A/B	B0(0)	B1(1)	B2(2)
A0(0)	**0**	**1**	**2**
A1(1)	**1**	**2**	**0**
A2(2)	**2**	**0**	**1**

A **A^1** **A^2**

Carry

A/B	B0(0)	B1(1)	B2(2)
A0(0)	**0**	**0**	**0**
A1(1)	**0**	**0**	**1**
A2(2)	**0**	**1**	**1**

1.Āp **1.Ān**

The Ternary Half Adder circuit as shown in Figure 2.

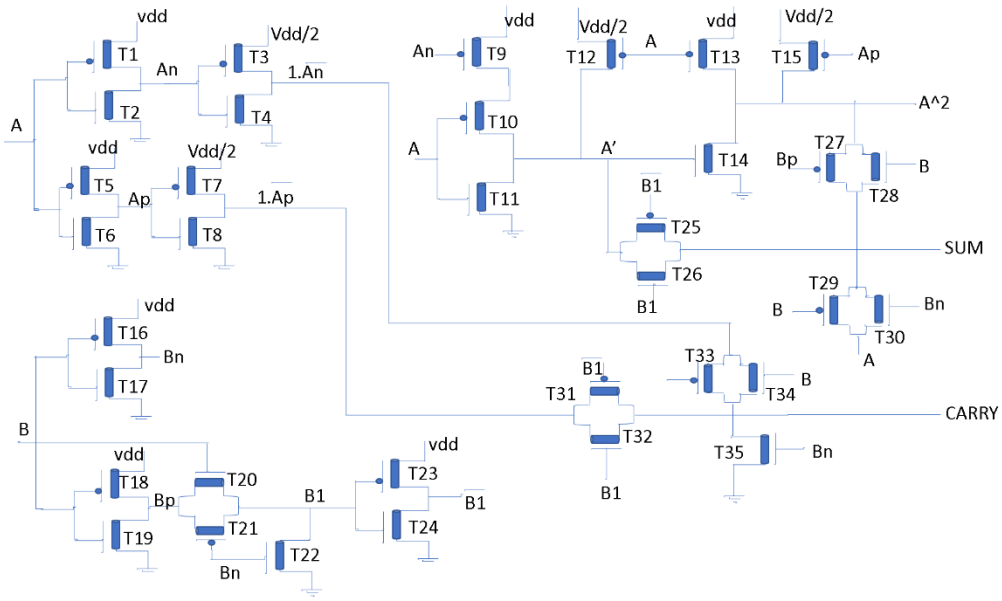

Fig 3. CNTFET based Ternary Half Adder

For CNTFET based Ternary Half Adder, the transistors diameters and their corresponding threshold voltages are in Table 4.

Table 4.THA threshold voltages for CNTFET

Transistors	**Diameter(nm)**	**Threshold voltage(v)**
T3,T5,T7,T9,T10 T15,T18,T21	1.487	-0.289
T11,T12,T13,T16,T23, T25,T27,T29,T31,T33	0.783	-0.559
T2,T17,T20	1.487	0.289
T4,T11,T14,T19,T22,T24,T26,T28 ,T30,T32T34,T35	0.783	0.559

Figure 3 shows the proposed THA with 35 CNTFETs using unary operators, transmission gates (TGs), and dual-voltages (Vdd, Vdd/2). Without using cascading TGs, which is the advantage compared to THA with 34 CNTFETs in that used cascading TGs. Because cascading TGs provide higher propagation delays and energy consumption. When the voltage supply (Vdd) decreases in a transistor then the propagation delay will increase. Therefore, any path from inputs to outputs contains transistors that have voltage supply equal to Vdd/2, that path will have higher propagation than other paths that have voltage supply equal Vdd. The Propagation delay of Ternary Half Adder is in Table 4.

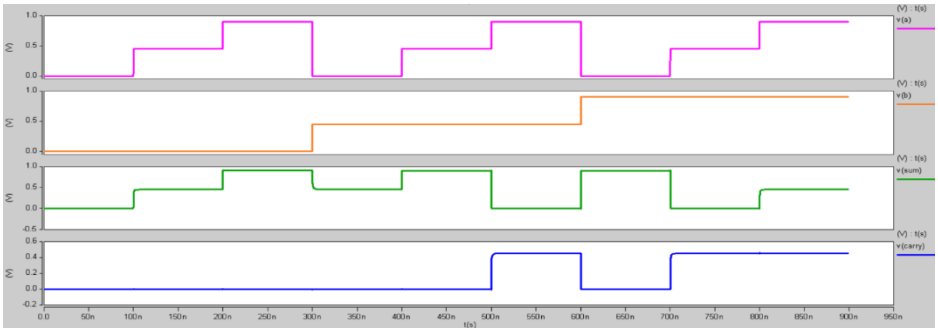

Fig4. Simulated output of Ternary Half Adder CNTFET

Replace the CNTFET transistorsin the Figure 10 with the GNRFET with supply voltage (vdd)1.2 V . The transistorsdimer lines and their corresponding threshold voltages are in Table 5.

Table 5. THA threshold voltages for GNRFET

Transistors	Dimer Lines(N)	Threshold voltage(v)
T3,T5,T7,T9,T10 T15,T18,T21	12	-0.289
T1,T12,T13,T16,T23,T25,T27,T29,T31,T33	7	-0.559
T2,T17,T20	12	0.289
T4,T6,T8,T11,T14,T19,T22,T24,T26,T28,T30,T32,T34,T35	7	0.559
T13	6	-0.428

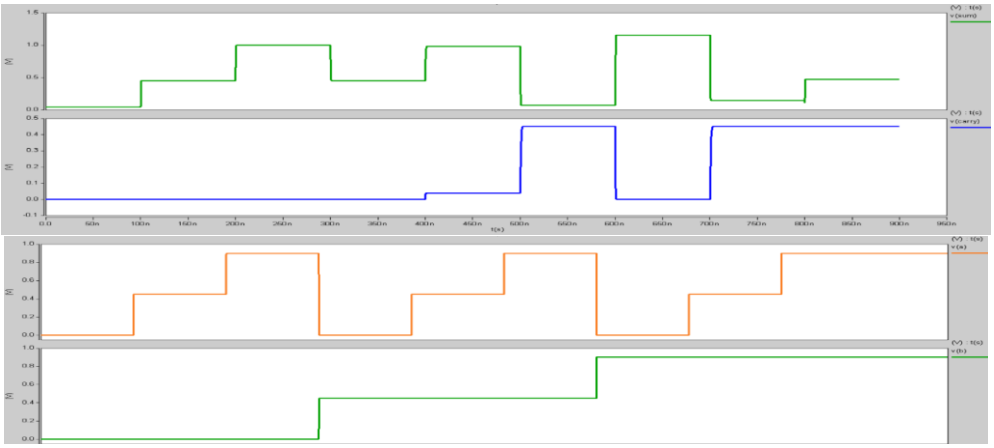

Fig 5. Simulated outputof Ternary Half Adder GNRFET

Comparison of Power, delay, power-delay product (PDP) of CNTFET based Ternary Half Adder and GNRFET based Ternary Half Adder is shown the Table 6.

Table 6: THA comparison

	Power(µw)	**Delay(ps)**	**PDP× 10^{-18}**
CNTFET-THA	13.46	16.92	227.7
GNRFET-THA	97	2.9	281.3

Ternary Multiplier

The multiplier circuit has two input variables and two output variables. The input variables are the cumulative number and the output variables are product and carry. Table 7 shows the Truth table of Ternary multiplier.

Table 7. Truth table of Ternary Multiplier

A	B	Carry	Product
0	0	0	0
0	1	0	0
0	2	0	0
1	0	0	0
1	1	0	1
1	2	0	2
2	0	0	0
2	1	0	2
2	2	1	1

The mathematical expression of product and carry for ternary multiplier can be obtained from Table 14 are given below.

$$\text{Product} = 2 .(A_1B_2 + A_2B_1) + 1 .(A_1B_1 + A_2B_2)$$

$$\text{Carry} = 1 . (A_2B_2)$$

The above truth table can be also represent as shown in Table 8 and Table 9.

Table 8. Modified Truth table for product

A/B	B0(0)	B1(1)	B2(2)
A0(0)	**0**	**1**	**0**
A1(1)	**1**	**2** A	**2** A²
A2(2)	**2**	**0**	**1**

Table 9. Modified Truth table for carry

A/B	B0(0)	B1(1)	B2(2)
A0(0)	0	0	0
A1(1)	0	0	0
A2(2)	0	0	1

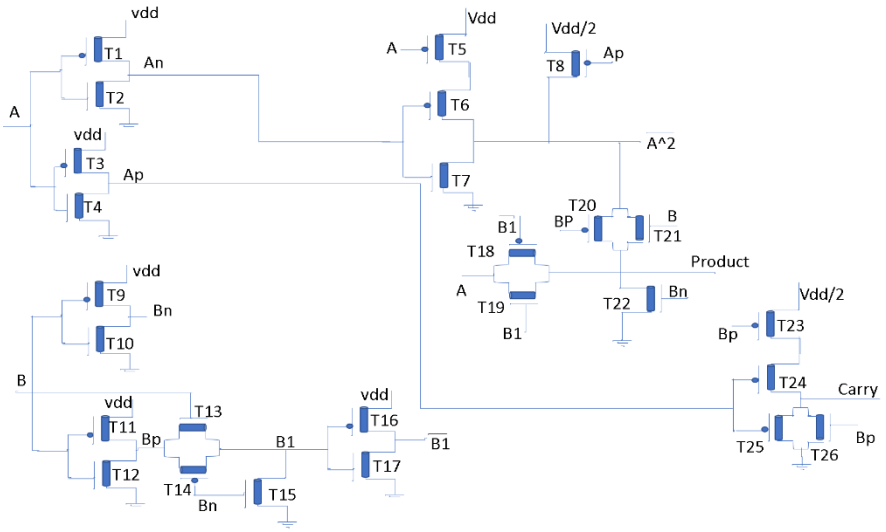

Fig 6. CNTFET based Ternary Multiplier

For CNTFET based Ternary Multiplier, the CNTFET transistors diameters and GNRFET transistors dimer lines and their corresponding threshold voltages are in Table 10.

Table10. Ternary multiplier parameters of CNTFET and GNRFET

Transistors	**Diameter(nm)**	**Dimer lines (N)**	**Threshold voltage(v)**
T3,T5,T8,T11,T14,T23,T24	1.487	12	-0.289
T1,T6,T9,T16,T18,T20,T25	0.783	7	-0.559
T2,T10,T13	1.487	12	0.289
T4,T7,T12,T15,T17,T19,T21, T22,T26	0.783	7	0.559

Fig 7 shows theTMUL with 26 CNTFETs using four unary operators, transmission gates (TGs), and dual-voltages (Vdd, Vdd/2).

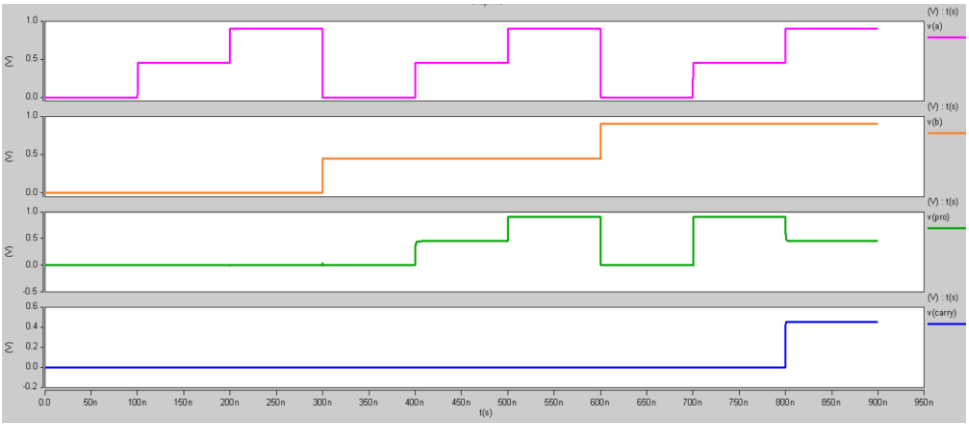

Fig 7. Simulated results of TernaryMultiplier CNTFET

Figure 8 shows the proposed TMUL with 26 CNTFETs using four unary operators, transmission gates (TGs), and dual-voltages (Vdd, Vdd/2).

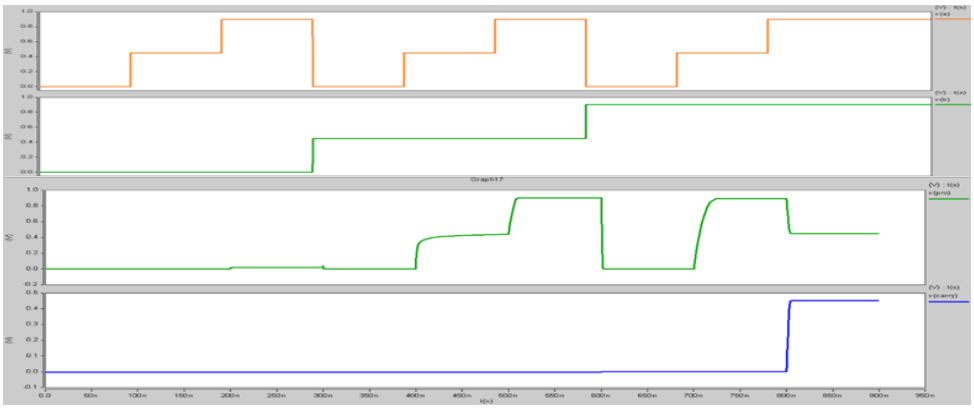

Fig 8. Simulated results of TernaryMultiplier GNRFET

Comparison of Power, delay, power-delay product(PDP) of CNTFET based Ternary Multiplier and GNRFET based Ternary Multiplier is shown the Table 11.

Table 11: Comparison of Delay and power of THA

	Power(µw)	**Delay(ns)**	**PDP× 10^{-15}**
CNTFET-Tmul	0.41	300.0	1.2
GNRFET-Tmul	19	300.0	57

Voltage Variations

This paper analyses and simulates the proposed and all the investigated THAs and TMULs for Voltage variations. The proposed circuits and all the investigated circuits simulated with voltage variations (from 0.8V to 1V).The results are as shown in Figure 16.

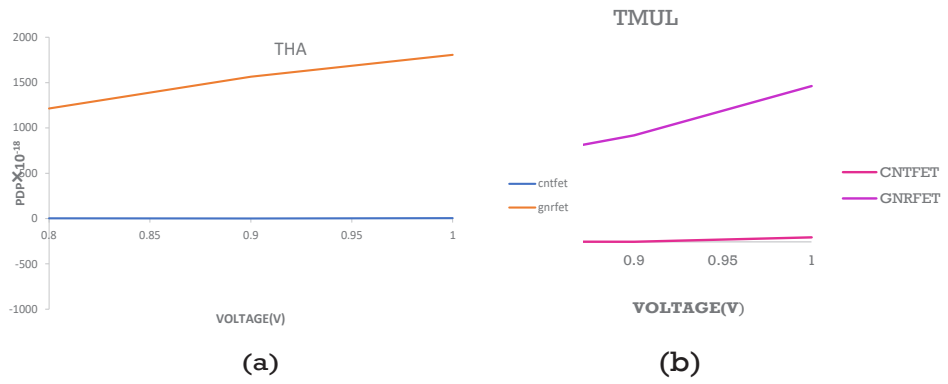

Fig 9. Simulated outputs of (a) Ternary Half Adder (b) Ternary Multiplier

Less change in PDP when change in voltage in CNTFET-based circuits. Where as there is more change in PDP in GNRFET-based circuits when change in voltage.

Conclusion

This work presented a Nano transistor based digital circuits to improve the performance of the digital circuits and proposed novel designs of 32 nm GNRFET-Based Ternary Half Adder and Ternary Multiplier using proposed Unary Operators combined with transmission gates with out using ternary decoders, basic logic gates, or ternary encoders. And the comparison of the effect of CNTFET and GNRFET parametric variation with threshold voltage on performance metrics namely delay and power has been analyzed. In CNTFET threshold voltage can be controlled by diameter which depends on the chirality vector. In GNRFET threshold voltage can be controlled by width which depends on number of dimer lines. The design process utilizes different techniques in terms of transistor arrangement, two power supplies (Vdd, Vdd/2), transistor count reduction to reach the final target. The Ternary Half Adder and Ternary Multiplier are designed using industry standard HSPICE to achieve propagation delay and power. Finally, the proposed THA and TMUL can be implemented in low-power nano-scale embedded systems and IoT devices to save battery consumption.

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