Performance analysis of 4-bit ternary adder and multiplier using CNTFET for high speed arithmetic circuits

Venkataiah C[1*], *Mallikarjuna Rao*Y[2], *Manjula* Jayamma[3], *Rambabu* S[2], *Linga Murthy* MK[4], *Laith H.* Alzubaidi[5], *Sanjay* Mishra[6]

[1*]Rajeev Gandhi Memorial College of Engineering and Technology, Nandyal, India.
[2]Santhiram Engineering College, Nandyal, Andhra Pradesh-518501, India
[3]SVR Engineering College, Nandyal, Andhra Pradesh-518501, India
[4]Sr.Assistant Professor, ECE Department, Lakireddy Bali Reddy College of Engineering (Autonomous), Mylavaram, Krishna District-521230, Andhra Pradesh, INDIA
[5]The Islamic University, Faculty of Engineering, Najaf, Iraq
[6] Uttaranchal School of Computing Sciences, Uttaranchal University, Dehradun 248007 INDIA

Abstract: Multiple valued logic (MVL) can represent an exponentially higher number of data/information compared to the binary logic for the same number of logic bits. Compared to the conventional devices, the emerging device technologies such as Graphene Nano Ribbon Field Effect Transistor (GNRFET) and carbon nanotube field effect transistor (CNTFET) appears to be very promising for designing MVL logic gates and arithmetic circuits due to some exceptional electrical properties such as the ability to control the threshold voltage. This variation of the threshold voltage is one of the prescribed techniques to achieve multiple voltage levels to implement the MVL circuit.This work presents a 4-input ternary adder using carbon nanotube field effect transistor (CNTFET). Many researchers have been done work on implementation of ternary adders and multipliers. But no one has done the comparison of this proposed ternary adder with different types of nano transistors. Hence this work has been proposed a design of low power and high speed 4-input adder which will be useful for designing of fast ternary multipliers. All the proposed designs have been simulated using emerging device such as CNTFET at 32nm technology node. From the simulations, we have calculated the power consumptions of the proposed designs, carry propagation delay and power delay product for the CNTFET circuits. It has been observed that CNTFET based proposed logic circuits given a better performance than the conventional logical circuits.

Key words: Carbon nano-tube field effect transistor (CNTFET), Power consumption, Ternary logic circuits, Ternary adders and multipliers.

* Corresponding Author: venki.challa@gmail.com

1. Introduction:

Multiple Valued Logic (MVL) and its' applications have been studied extensively over the last couple of decades due to the ability of the MVL logic devices to provide an exponentially
higher information density compared to the binary logic. In Binary or Boolean logic system (base 2), each logic bit can have two possible values: low (0) and high (1). Whereas, in the MVL system (base 3 or more), each digit can have three or more possible values leading to significantly higher information density with smaller logic gates and reduced circuit complexity. As a result, the energy consumption, area, and circuit overheads and other costs for each bit of information would decrease in the MVL system [1]. For example, in the ternary logic system, it takes only log32n bits to represent an n-bit binary number [2], which reduces the computational complexity to a large extent and thus enhances the power and area efficiency of the system. Multiple valued logic can be ternary (radix 3), quaternary (radix 4), quinary (radix 5), etc. However, ternary and quaternary logic systems have drawn much attention from the research community. The ternary logic system appears to be the most feasible MVL system that can be adopted in the near future because of its simplicity and ease in distinguishing different logic levels as in the binary system. At smaller technology nodes, the supply voltage is limited to a value equal to or less than 1.2 V. Therefore, a higher number of discrete voltage levels needed to identify different logic values within this limited supply range (0 to 1.2 V) would be challenging and susceptible to noise and other signal integrity issues. As a consequence, most of the recent research workfocuses on ternary logic and memory. The initial efforts toimplement ternary logic are based on the prevailing CMOS and other technologies available since 1974 [3-5]. Dueto short channel effects, scaling limitations, DIBL, energyconsumption, and other signal integrity issues, conventionaltechnologies are not appealing for the MVL system. Newmaterials and new device technologies like carbon-basedFETs, QDGFET, and Memristor [6-8] are being explored to overcome these limitations and implement reliable MVL circuits.

Carbon-based Field Effect Transistors (FETs) are drawing widespread attention due to their outstanding electrical properties and integration capabilities. Carbon-Nano-Tube-Field- Effect-Transistor (CNTFET) and Graphene-Nano-Ribbon- Field-Effect-Transistor (GNRFET) are the two forms of carbon-based transistor that have become trendy research topics. Different pieces of literature are found which work in CNTFET and GNRFET based ternary logic design [9-21] which uses the threshold voltage control method for implementing different ternary logic circuits and arithmetic circuits. Generally binary adders add 3 inputs to give sum and carry. But in ternary logics we can add 4 inputs at a time to produce final sum and carry which will reduce the number of stages in the Wallace tree multiplier.In this paper, we present a design approach for CNTFET based ternary logic circuits because of low supply voltage and multi threshold voltage

2. Ternary adders and simulation outputs:

The sum output is generated using a ternary XOR gate. When both inputs are 0 or both inputs are 2, the output of the XOR gate is 0. When one input is 0 and the other input is 1, or oneinput is 1 and the other input is 2, the output of the XOR gate is 1. When one input is 0 and the other input is 2, or both inputs are 1, the output of the XOR gate is 2.The carry output is generated using a ternary AND gate. When both inputs are 0 or one input is 0 and the other input is 1, the output of the AND gate is 0. When one input is 2 and the other input is 1 or both inputs are 2, the output of the AND gate is 2. When both inputs are 1, the

output of the AND gate is 1.If the sum output of the ternary half-adder is 2, then a carry has been generated and it needs to be propagated to the next higher-order digit.

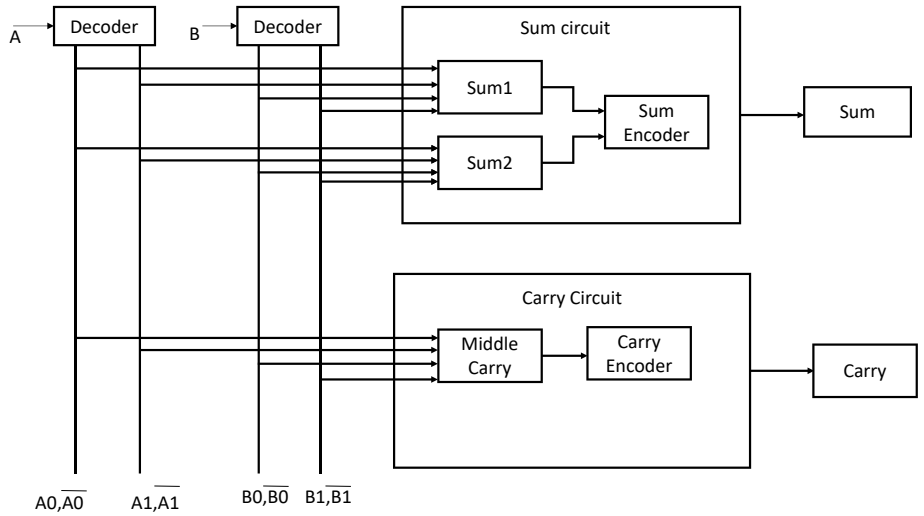


Fig 1: Block diagram of Ternary half adder

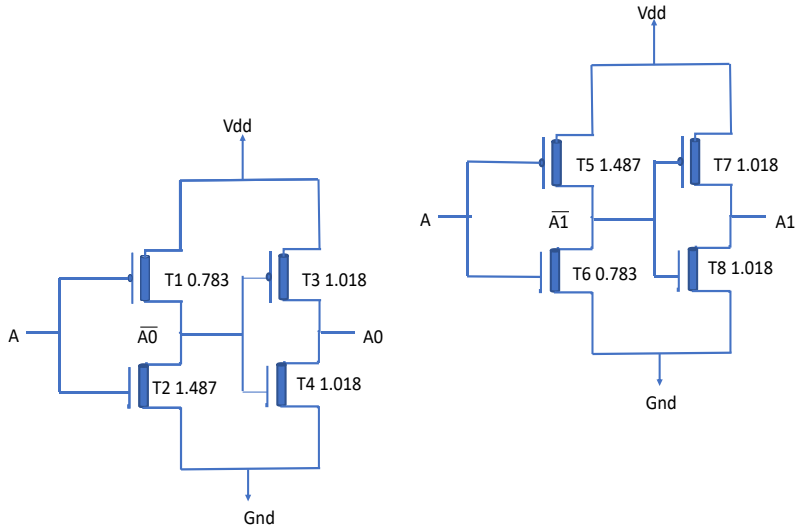


Fig 2: Decoder Circuit

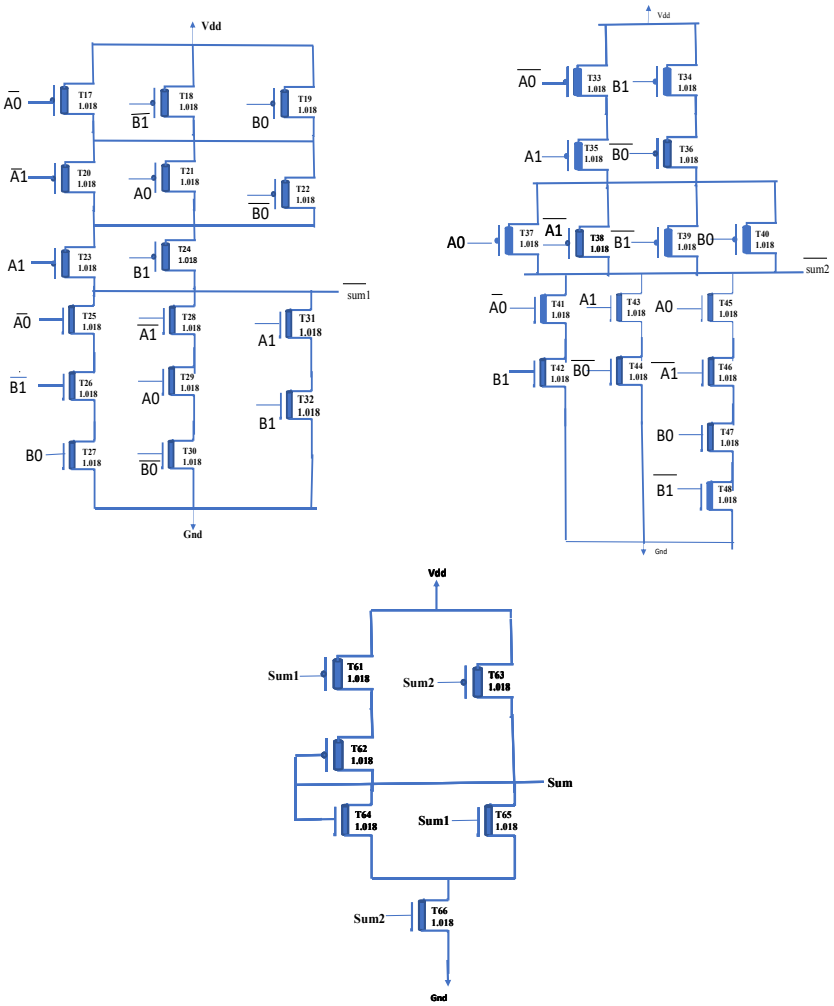


Fig 3: Sum circuit

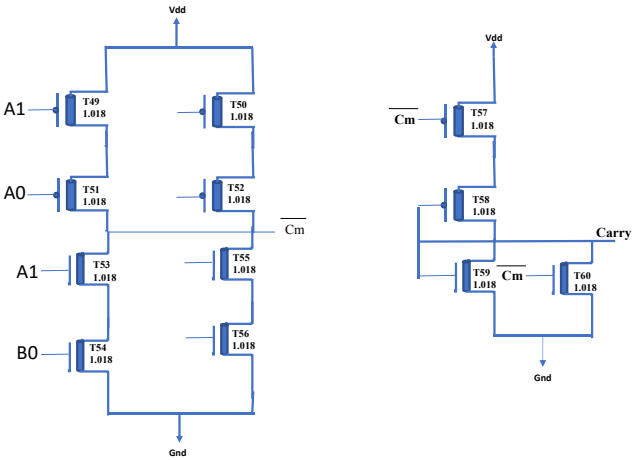


Fig 4:Carry generation

Table1: Truth table for THA

A	B	Sum	Carry
0	0	0	0
0	1	1	0
0	2	2	0
1	0	1	0
1	1	2	1
1	2	0	2
2	0	2	0
2	1	0	2
2	2	1	2

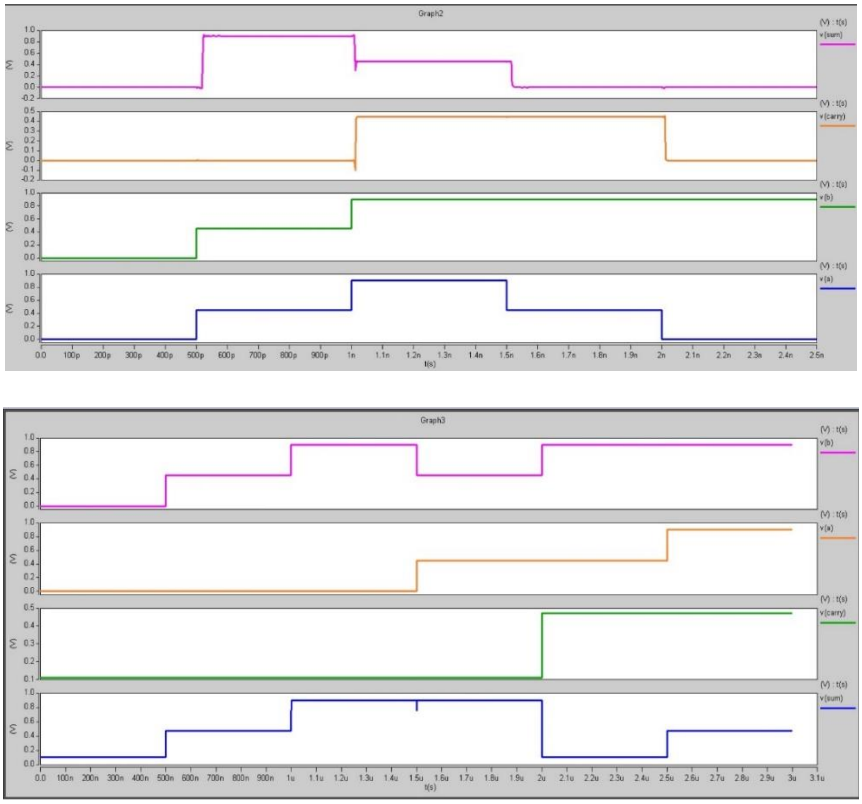


Fig 5: Simulated outputs of ternary half adder

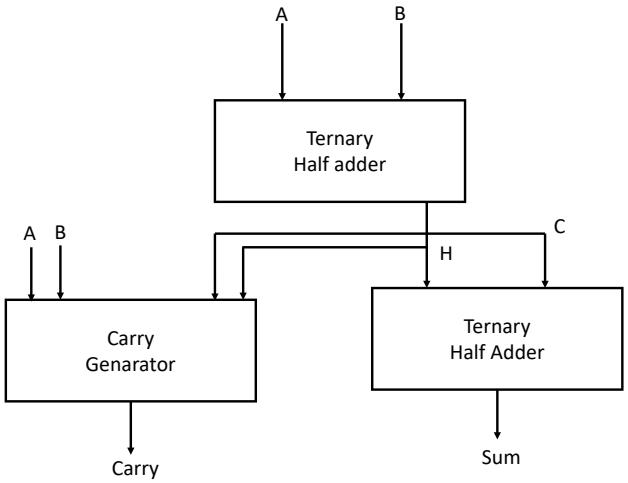


Fig 6: Block diagram for Ternary full adder

Table2: Truth table for THA

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	0	2	2	0
0	1	0	1	0
0	1	1	2	0
0	1	2	0	1
0	2	0	2	0
0	2	1	0	1
0	2	2	1	1
1	0	0	1	0
1	0	1	2	0
1	0	2	0	1
1	1	0	2	0
1	1	1	0	1
1	1	2	1	1
1	2	0	0	1
1	2	1	1	1
1	2	2	2	1
2	0	0	2	0
2	0	1	0	1
2	0	2	1	1
2	1	0	0	1
2	1	1	1	1
2	1	2	2	1

2	2	0	1	1
2	2	1	2	1
2	2	2	0	2

In the above table, the input digits A, B, and C represent the digits being added, and produce the sum and carry respectively. For each input combination of A, B, and C, the ternary full-adder performs the following steps:Add A and B to produce a temporary sum T.Add T and C to produce the final sum S.Determine the carry by checking if the sum S is greater than or equal to 3.If S is 3 or more, then there is a carry is 1.In general, when all three inputs of a ternary full-adder are the same, the carry out will be equal to 1 if the input is 2 or greater, and equal to 0 if the input is 0 or 1. The sum output will be 0 in all cases.

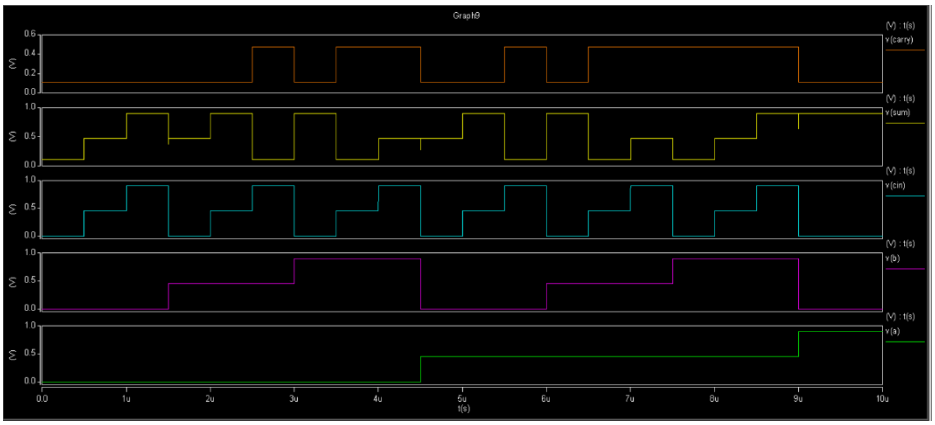


Fig 7: Simulation outputs of TFA

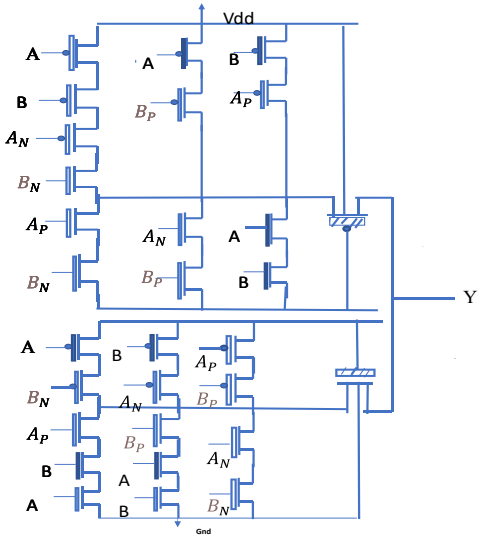


Fig 8: Sum Logic circuit

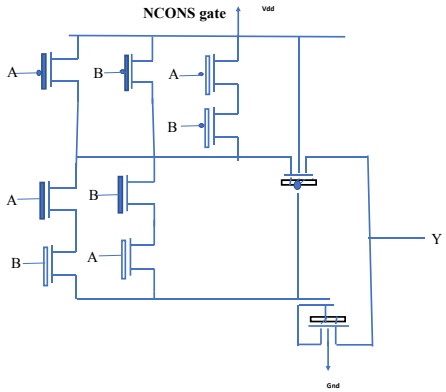


Fig 9: Cons logic circuit

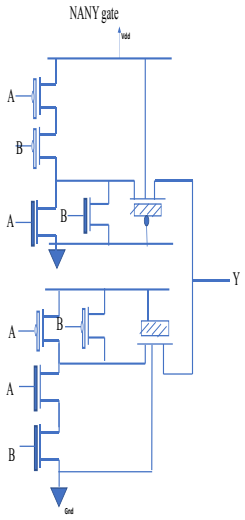


Fig 10: ANY logic circuit

Table 3: Truth table for SUM, CONS, ANY circuit

Sum	0	1	2
0	0	1	2
1	1	2	0
2	2	0	1

Cons	0	1	2
0	0	0	0
1	0	0	1
2	0	1	1

Any	0	1	2
0	0	1	1
1	1	2	2
2	1	2	2

The number of transistors used for SUM gate is 30, and additional eight transistors are used for NTI and PTI logic circuits. The transistor count of the NCONS gate is 10 and 6 transistors for inverter.The transistor count of the NANY gate is 10 and 6 transistors for inverter.SUM subcircuit output is sum bit of adder represented in ternary system. CONS subcircuit output is high when at least one output is high.ANY subcircuit output is logic '2' when both inputs are logic'1' and when atleast one input is logic'2'. For logic ‘0’ input , the N type CNTFETs are turned ON in the both pull-up and pull-down network.For logic ‘2’ input , the P type CNTFETs are turned ON in the both pull-up and pull-down network.For logic ‘1’ input , the P type CNTFETs of pull-down network and N type of pull up network are turned ON.Pass transistors are always turned ON in all the cases.

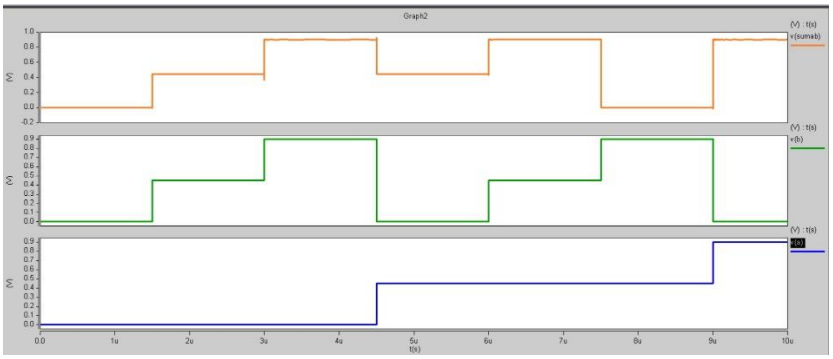


Fig 11: Simulation outputs of Sum

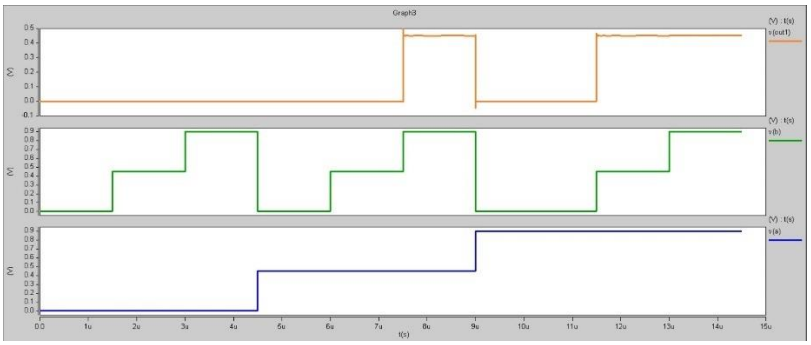


Fig 12: Simulation output of Cons

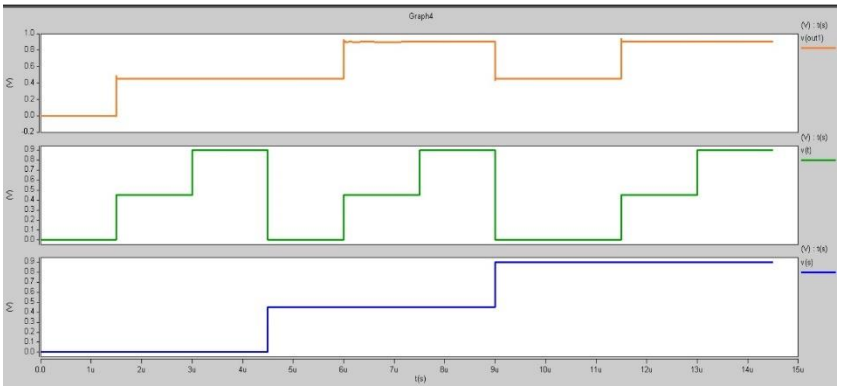


Fig 13: Simulation output of ANY

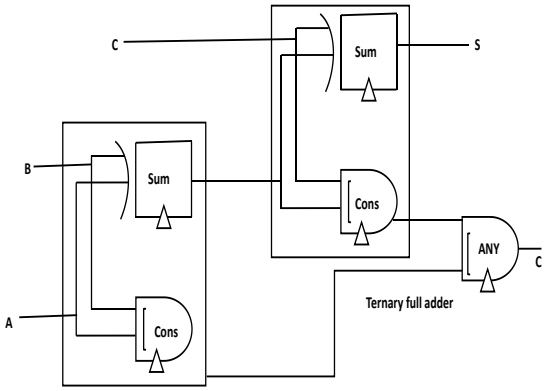


Fig 14: Block diagram of 3 input ternary full adder

3-input Ternary adder is combination of 2 Ternary Half adders. The design contains the 2 SUM, 2 CONS and 1 ANY subcircuits.

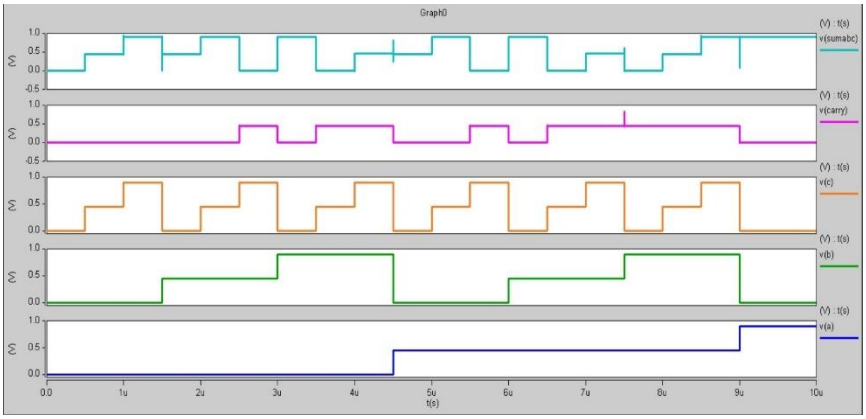


Fig 15: Simulation output of 3 input Ternary adder

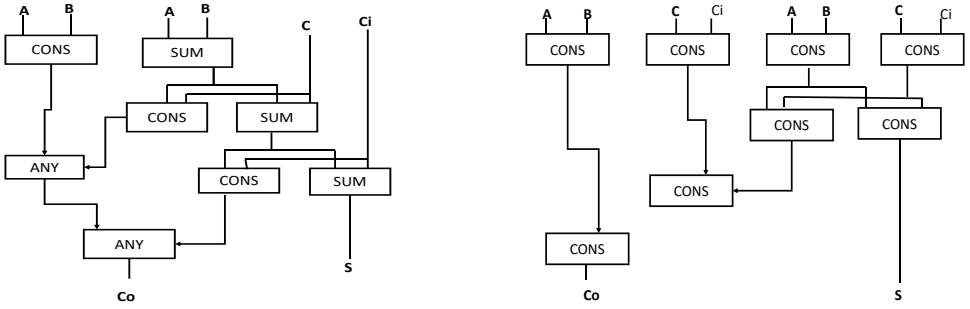


Fig 16: Block diagram of 4 input ternary full adder

We designed Half adder , 3 input Full adder and 4 input Full adder using SUM , CONS and ANY gates. The total transistor count of the ternary 3 input ternary full adder is 124 , and total transistor count of the 4 input ternary full adder is 194.In the 4 input ternary adder. In the first design(TA) , first two inputs are added and then the sum of first two inputs is

added to third input . The total resultant is then added to the fourth input to give the final sum.In this design , even all the inputs are available in the begining stage , we are adding only one input in each stage similar to the conventional method.This will result in more delay .To overcome the above we proposed the second design. In the second design(TC), the four inputs are added with two SUM logic seperatly in the first stage itself and the generated two sums are added with another SUM logic.By this method the is reduced.The advantage of ternary adders over the binary adders is we can process 4 inputs at a time instead of 3 inputs so that the delay can be decreased.

This proposed 4-input adder will be used in many ternary multiplier applications. The partial products generated in the multipliers are added by proposed ternary adders to generate the accumulate. The generated accumulates are furthur added with fast ternary adders to generate final result.
We have also designed 4*4 bit multiplier using proposed adder. First the partial products are obtained using the 1-bit multiplier. The generated partial products are grouped and added with 2-input,3- input, 4-input proposed Ternary adders to generate accumulate. The accumulate is then added with Fast ternary adder to give final result. In the normal conventional method we use to add only two/three inputs to generate the accumulate. In the proposed system can add upto 4-inputs at a time.This will reduce the no.of stages in the multiplication process.As the no.of stages are reduced , the delay is also reduced.

5. Results analysis:

Here are the simulation results of the SUM, CONS, ANY, 3 input ternary adder, 4 input ternary adderand 4*4 Ternary Multiplier built with 32nm CNTFET technology.

Table 4: PDP table of ternary logic circuits

S.no	circuit	Load capacitor	Tr. Count	Avg. Power(µW)	Worst Delay (ns)	PDP (fJ)
1	SUM	2fF	38	0.202	0.05	0.01
2	CONS	2fF	16	0.11	0.022	0.0024
3	ANY	2fF	16	0.18	0.035	0.006

Table 5: Power , Delay , PDP of proposed Ternary Adders

S.no	circuit	Load capacitor	Tr. Count	Avg. Power (µW)	Worst Delay (ns)	PDP (fJ)
1	3 input TA	2fF	124	1.0	0.1	0.1
2	4 input TA	2fF	194	1.36	0.25	0.345
3	4 input TC	2fF	194	1.38	0.18	0.248

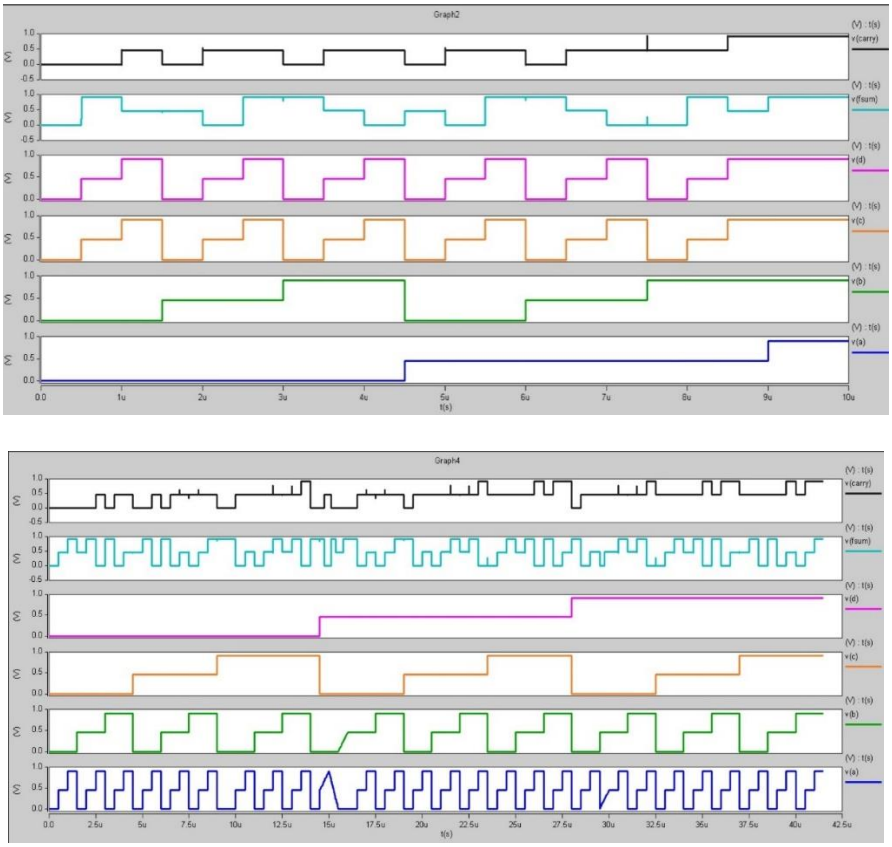


Fig 17: Simulation outputs for 4 input ternary adder

This proposed 4-input Ternary Full adder design having81 possible combinations. The power, delay and PDP is calculated by considering all 81 combinations. The power delay and PDP is compared with different designs and observed better improvement.The is power of proposed system is reduced by 93.75%, 83.06 %, 63.77%, 84.28%,64.61% in comparison with [1], [2], [3], [4], [6] respectively.The is delay of proposed system is reduced by 93.75%, 89.25 %,85.92% 64.66%, 90%, 74.1% in comparison with [1], [2], [3], [4], [5], [6] respectively.The power of proposed design is same as [5] but the delay is reduced to 90%.The is PDP of proposed system is reduced by 99.62%, 98 %, 94.88%, 94.2% ,90%,82.12% in comparison with [1], [2], [3], [4], [5], [6] respectively.

6. Design of multipliers

1 bit multiplier

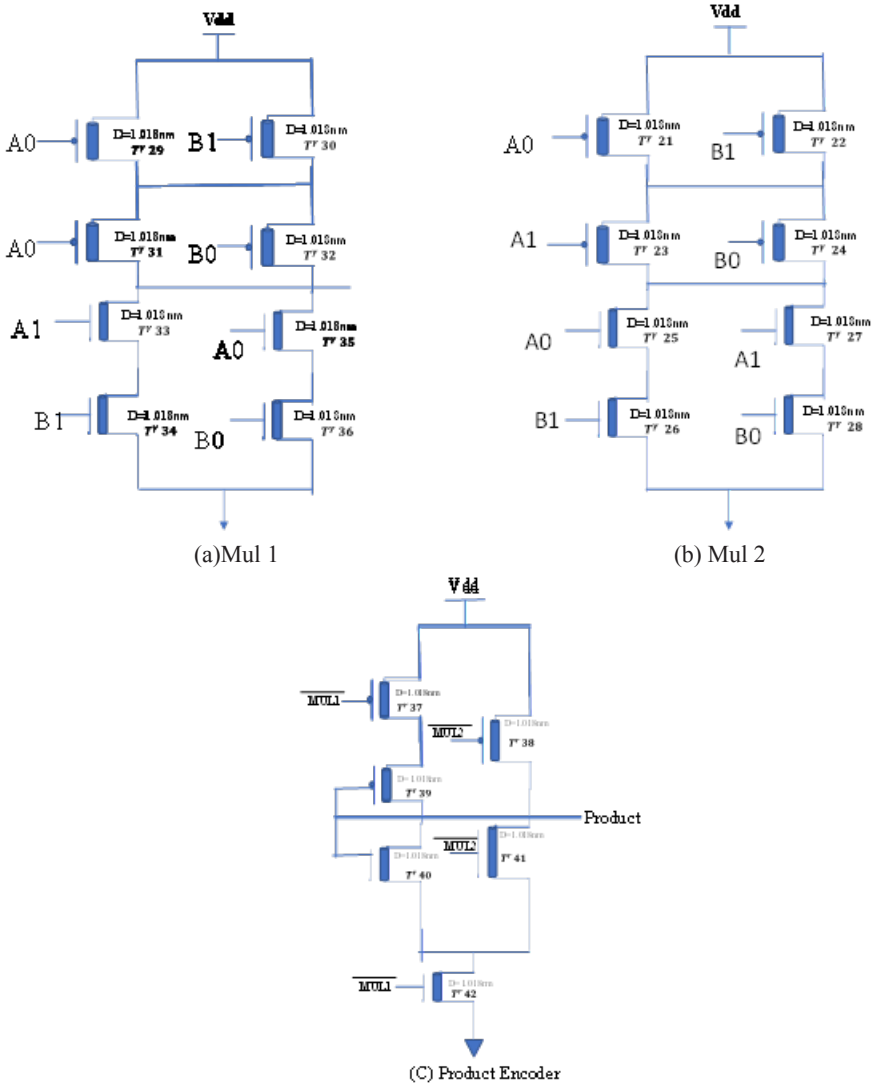
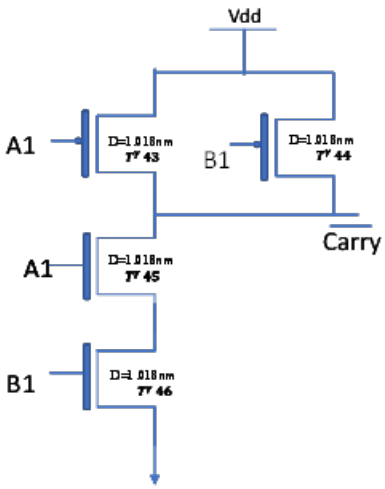
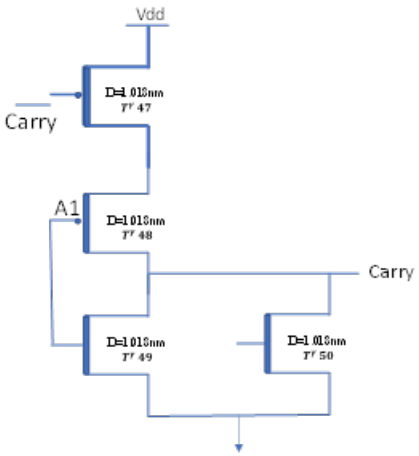


Fig 18: Sum generation



(d)Carry generator



(e)Carry encoder

Fig19: Carry generation

Table 6: Truth table for 1 bit multiplier

A	B	Product A*B	carry
0	0	0	0
0	1	0	0
0	2	0	0
1	0	0	0
1	1	1	0
1	2	2	0
2	0	0	0
2	1	2	0
2	2	1	1

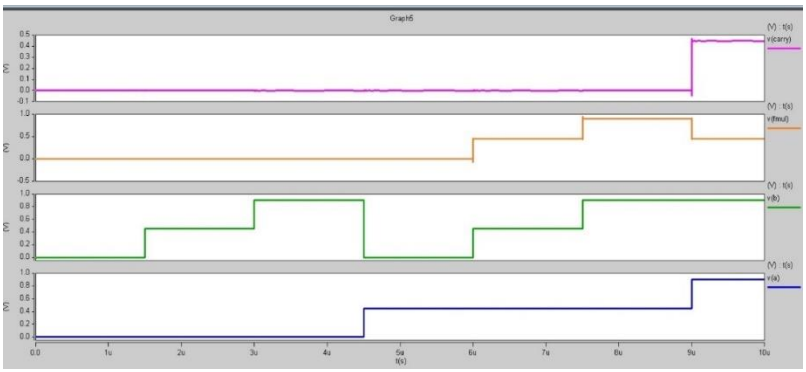


Fig 20: Simulation outputs for 1bit multiplier

Table 7: Power , Delay , PDP of 4*4 Ternary Multipliers

S.no	circuit	Load capacitor	Tr. Count	Avg. Power (µW)	Worst Delay (ns)	PDP (fJ)
1	4*4 ternary Multiplier	2fF	1676	8.34	960	15552

The 4 bit A input (a0 a1 a2 a3) is multiplied with 4 bit B (b0 b1 b2 b3 b4) input to generate the partial products and the partial products are added to generate final output (s0 s1 s2 s3 s4 s5 c6). The total transistor count for 4*4bit multiplier is 1676, Avg. Power is 8.34µ, delay is 960ns and PDP is 15552fJ.

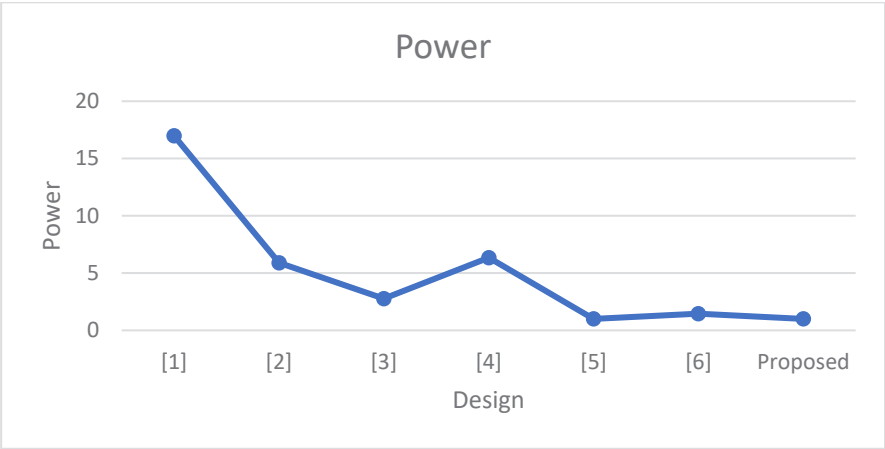


Fig 21: Comparison of Power of Ternary adder with different Designs

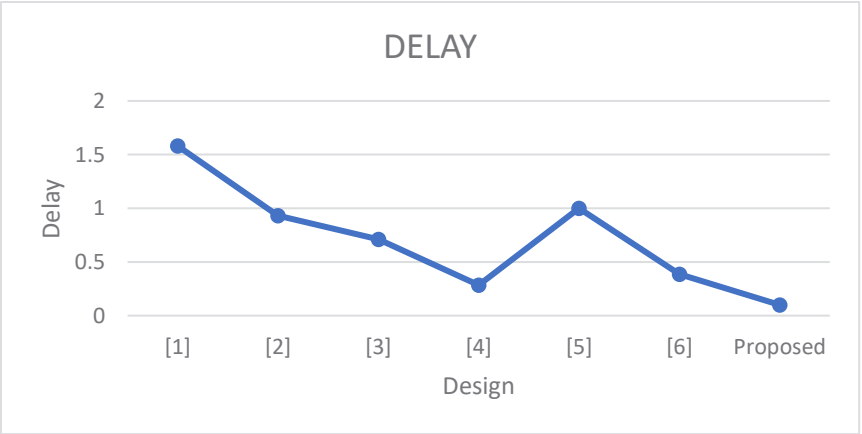


Fig 22 Comparison of Delay of Ternary adder with different Designs

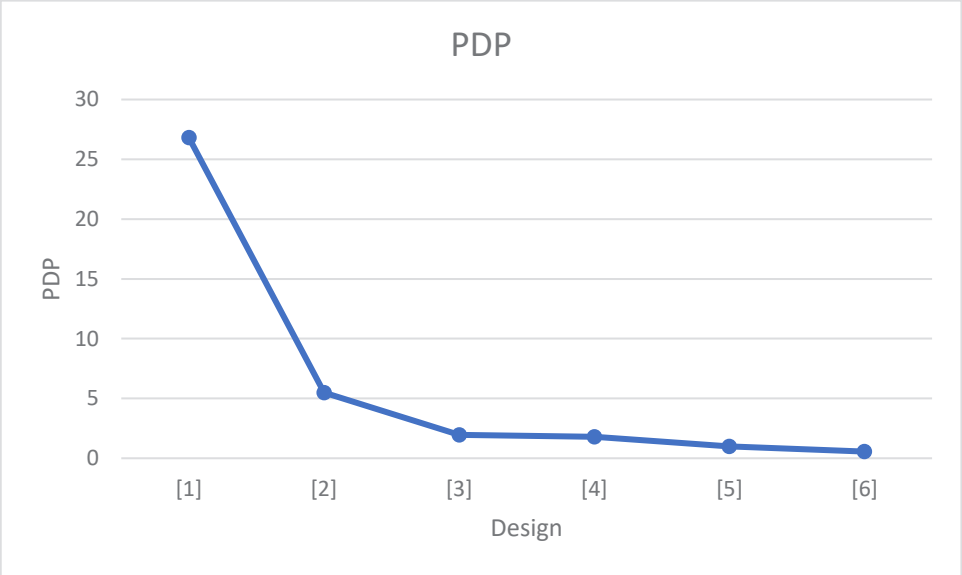


Fig 23: Comparison of PDP of Ternary adder with different Designs

Conclusion:

In this work, we have analysed the performance of the Ternary Adders and Ternary Multipliers which arebuilt by using the CNTFETs. Compared to the conventional devices, the emerging device technologies such as Graphene Nano Ribbon Field Effect Transistor (GNRFET) and carbon nanotube field effect transistor (CNTFET) appears to be very promising for designing MVL logic gates and arithmetic circuits due to some exceptional electrical properties such as the ability to control the threshold voltage. All the proposed deigns have been simulated at 32nm technology nodes. We have calculated the carry propagation delays, power dissipation and power delay product for all the proposed designs using CNTFET. It has been observed that CNTFET based proposed logic circuits given a better performance than the conventional logical circuits. Hence the proposed Ternary adder can be used in the multipliers for low power and high speed applications.

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